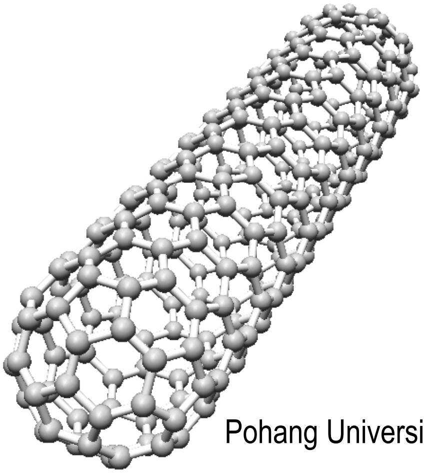
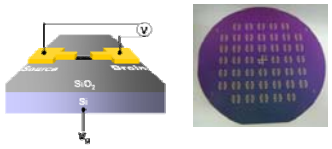
Sacrificing Carbon Nanotubes for the Fabrication of Nanostructures at Sub-10 nm Scale



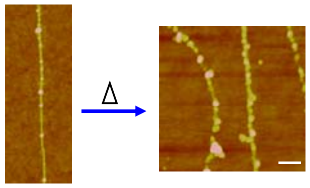
Hee Cheul Choi

Department of Chemistry,
Pohang University of Science and Technology (POSTECH)
South Korea, 790-784

Carbon nanotube platform for bio- and nanohybrid systems

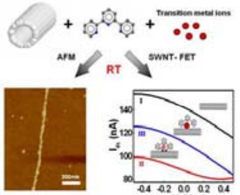


Nanoscale FET devices



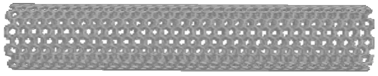
Choi, et al., *JACS* **2002**, 124, 9059.
Shin and Choi, et al., *Adv. Mater*. **2007**, In press.

Noble metal-SWNT composites



Lee and Choi, et al., *Small* **2005**, 1, 975.

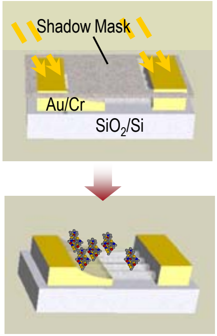
Transition metals

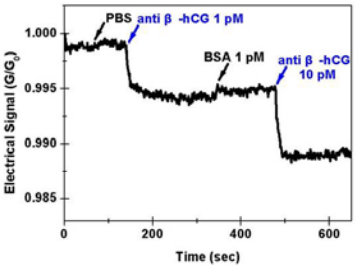


SWNT-Protein chip

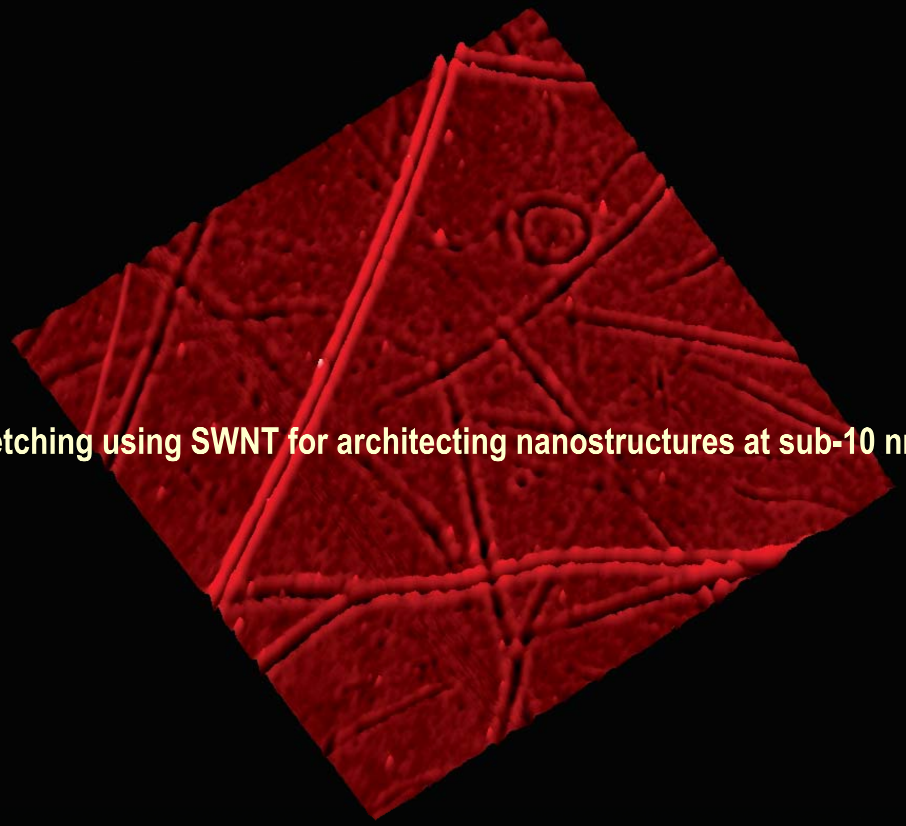
Byon and Choi, et al., *ChemBioChem* **2005**, 6, 1331.
Chi, Byon, Choi, Choi et al., *ChemBioChem* **2007**, submitted.

Ultra-high sensitive SWNT-FET biosensor





Chen and Choi, et al., *JACS* **2004**, 126, 1563
Byon and Choi *JACS* **2006,** 128, 2188



SiO$_2$ etching using SWNT for architecting nanostructures at sub-10 nm scale

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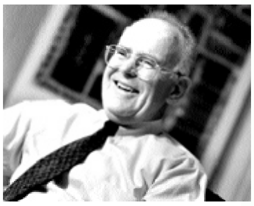
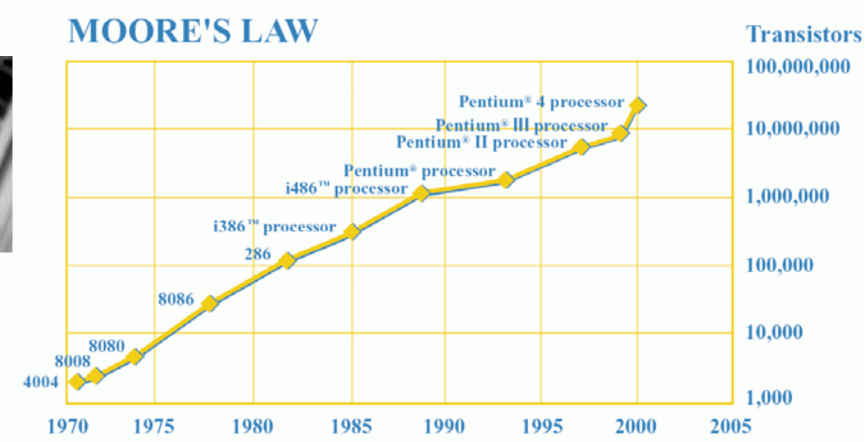
The birth of NanoScience

Moore's Law
- Performance of computer chips doubles about every 18 months



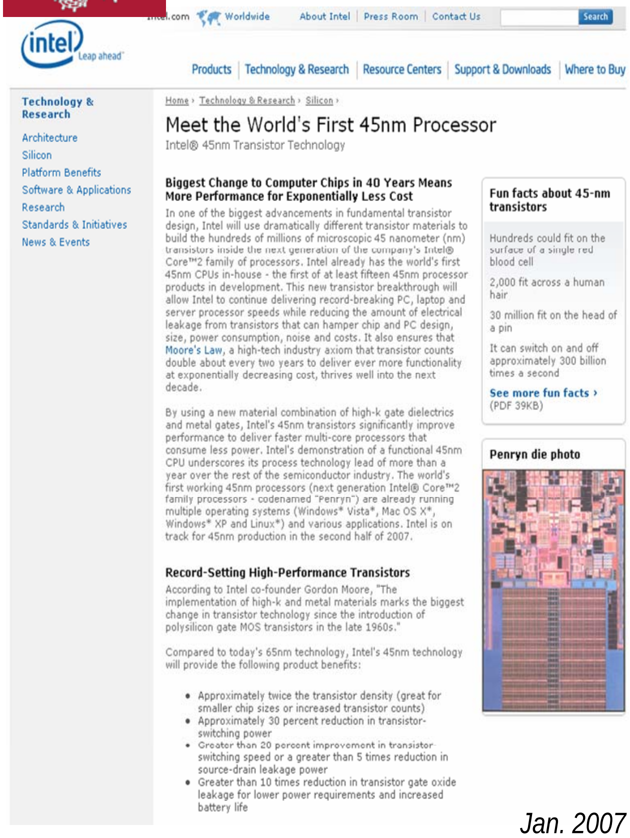
Gordon Moore, co-founder of Intel



Continuous development of lithographic techniques *vs.* molecular electronics

Candidates: carbon nanotubes, nanowires, single molecules, biomolecules, etc.

Intel® 45 nm Transistor Technology



Meet the World's First 45nm Processor

Intel® 45nm Transistor Technology

Biggest Change to Computer Chips in 40 Years Means More Performance for Exponentially Less Cost

In one of the biggest advancements in fundamental transistor design, Intel will use dramatically different transistor materials to build the hundreds of millions of microscopic 45 nanometer (nm) transistors inside the next generation of the company's Intel® Core™2 family of processors. Intel already has the world's first 45nm CPUs in-house - the first of at least fifteen 45nm processor products in development. This new transistor breakthrough will allow Intel to continue delivering record-breaking PC, laptop and server processor speeds while reducing the amount of electrical leakage from transistors that can hamper chip and PC design, size, power consumption, noise and costs. It also ensures that Moore's Law, a high-tech industry axiom that transistor counts double about every two years to deliver ever more functionality at exponentially decreasing cost, thrives well into the next decade.

By using a new material combination of high-k gate dielectrics and metal gates, Intel's 45nm transistors significantly improve performance to deliver faster multi-core processors that consume less power. Intel's demonstration of a functional 45nm CPU underscores its process technology lead of more than a year over the rest of the semiconductor industry. The world's first working 45nm processors (next generation Intel® Core™2 family processors - codenamed "Penryn") are already running multiple operating systems (Windows* Vista*, Mac OS X*, Windows* XP and Linux*) and various applications. Intel is on track for 45nm production in the second half of 2007.

Record-Setting High-Performance Transistors

According to Intel co-founder Gordon Moore, "The implementation of high-k and metal materials marks the biggest change in transistor technology since the introduction of polysilicon gate MOS transistors in the late 1960s."

Compared to today's 65nm technology, Intel's 45nm technology will provide the following product benefits:

- Approximately twice the transistor density (great for smaller chip sizes or increased transistor counts)
- Approximately 30 percent reduction in transistor-switching power
- Greater than 20 percent improvement in transistor-switching speed or a greater than 5 times reduction in source-drain leakage power
- Greater than 10 times reduction in transistor gate oxide leakage for lower power requirements and increased battery life

Fun facts about 45-nm transistors

Hundreds could fit on the surface of a single red blood cell

2,000 fit across a human hair

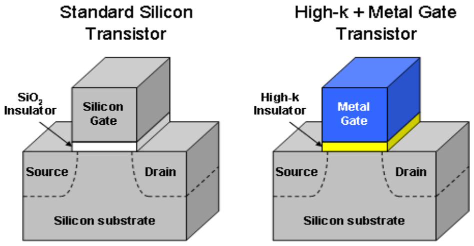
30 million fit on the head of a pin

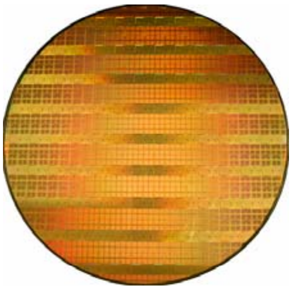
It can switch on and off approximately 300 billion times a second

See more fun facts ›
(PDF 39KB)

Penryn die photo

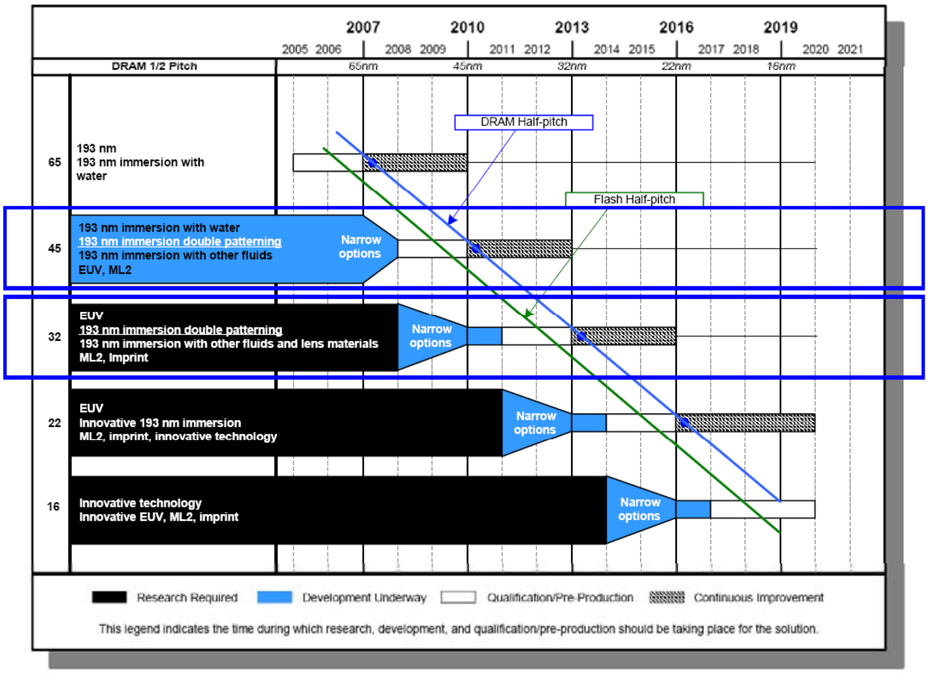
Intel Producing First Processor Prototypes With New,
Tiny 45 Nanometer Transistors,
Accelerating Era of Multi-Core Computing





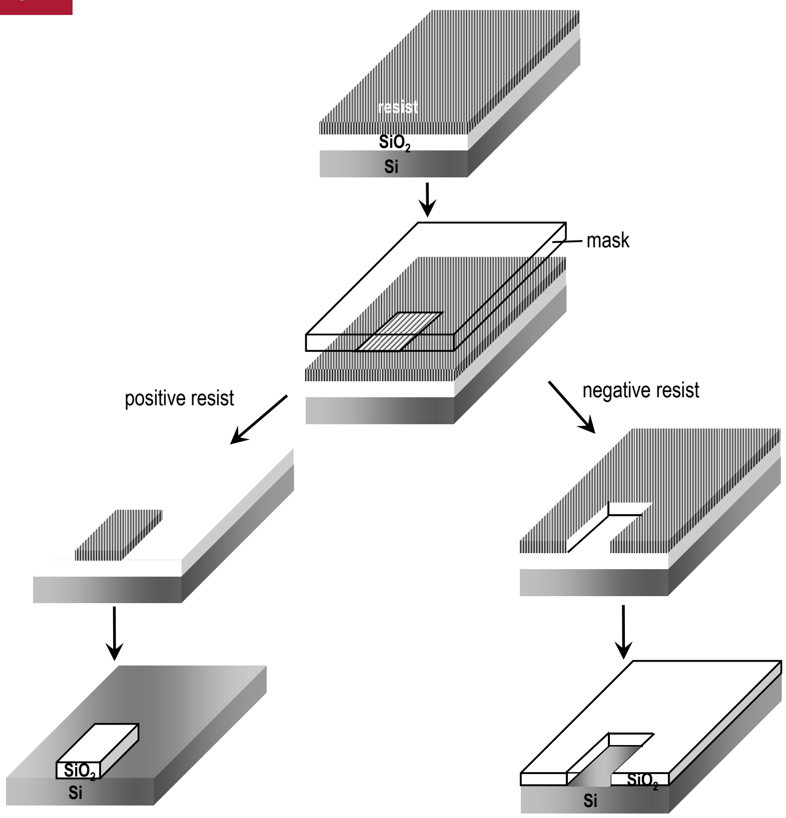
Jan. 2007 by Intel

Continuous progresses in lithography



Resource: 2006 ITRS, Lithography section

Conventional Lithography



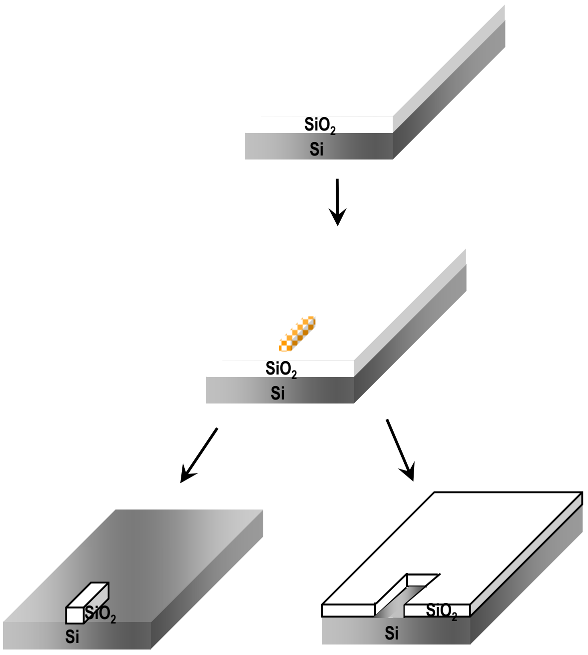
PR/ER Coating

Patterned Mask
+
Photon Energy (EUV or X-ray)

development

Etching

New Paradigm in Lithography



Patterned Nanostructures

Nanostructures induced
SiO_2 Reduction Reaction (Etching)

Carbon chemistry for high resolution lithography

“Carbothermal Reduction (SiO_2 etching)”

“Reduction of metal ions or metal oxide using carbons at high temperature”

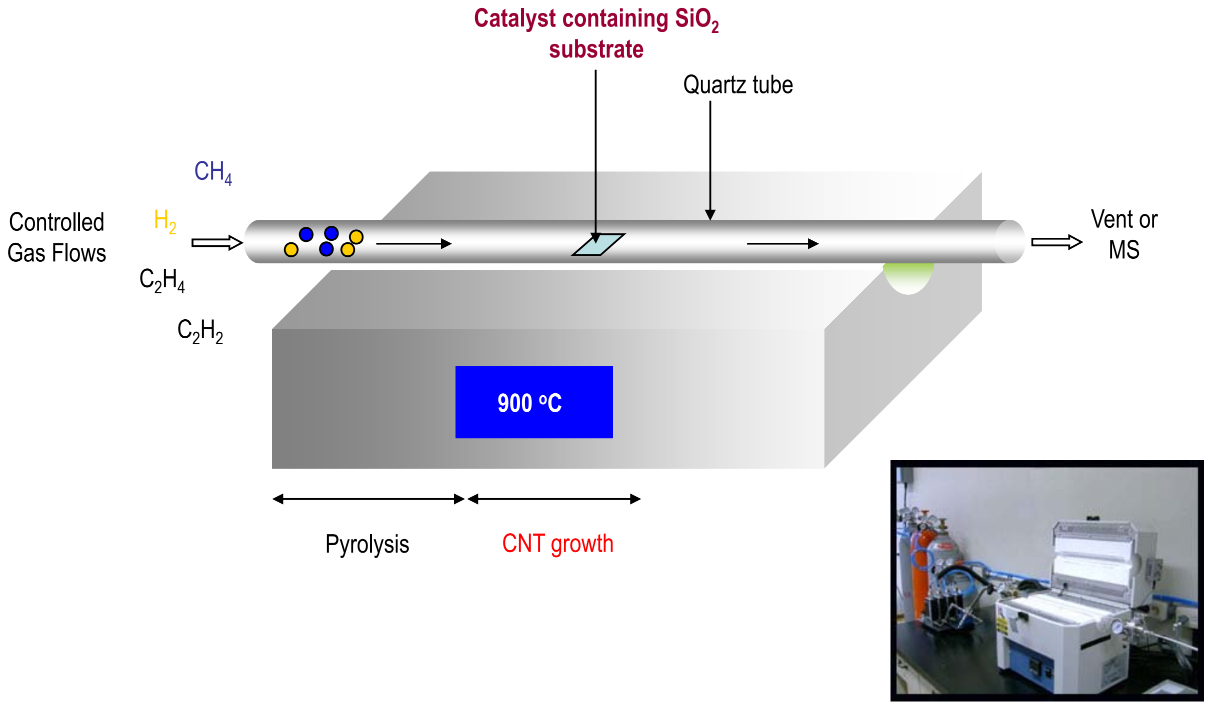
- General Chemistry Text book

$$\boxed{C(s) + SiO_2(s) \leftrightarrow CO(g) + SiO(g)}$$

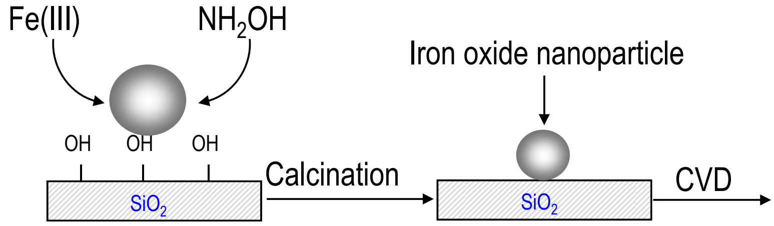
How about carbon nanotube with 1~3 nm of diameters
instead of micro/macro-scale carbon (graphite) powder?

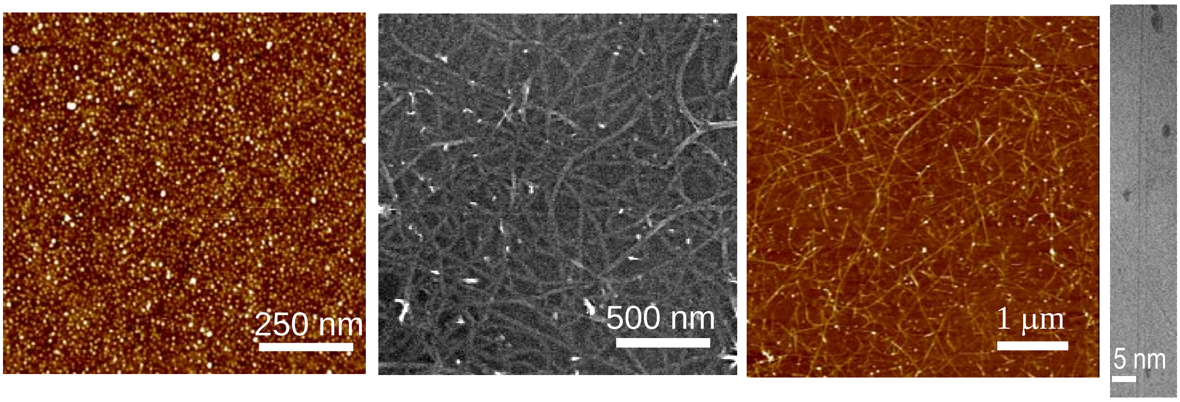
Is it going to occur for real?
What’s the difference to the conditions for the conventional carbon nanotube growth?

Synthesis of carbon nanotubes : Chemical Vapor Deposition (CVD)



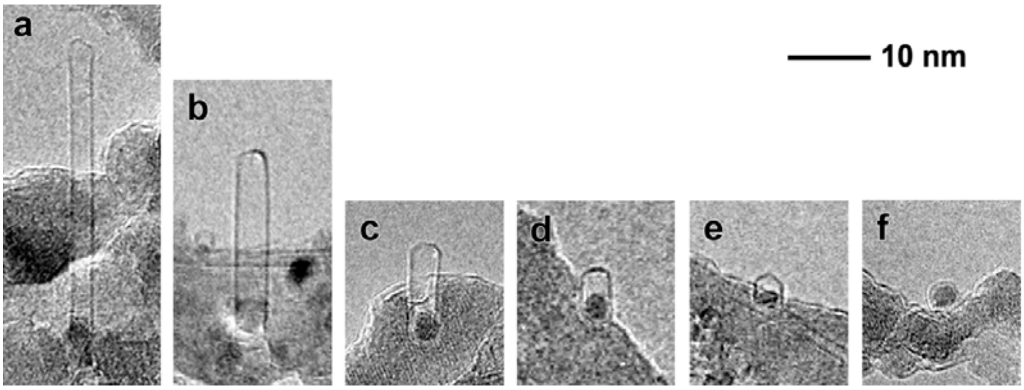
Fe catalyst nanoparticles, Hydrocarbon sources, and Carbon nanotubes





Choi, H. C. et al., *Nano. Lett*. **2003**, *3*, 157.

Fe nanoparticle-assisted growth of CNT



- Particle size is corresponding to the nanotube diameter
- Catalytic particles (active end) remain on support
- The other end is dome-closed
- Base growth (differs from the VLS growth mode)

Li, U. J. et al. *JPCB*. **2001**, *105*, 11424.

Carbon chemistry for high resolution lithography

“Carbothermal Reduction (SiO_2 etching)”

“Reduction of metal ions or metal oxide using carbons at high temperature”

- General Chemistry Text book

$$\boxed{C(s) + SiO_2(s) \leftrightarrow CO(g) + SiO(g)}$$

How about carbon nanotube with 1~3 nm of diameters instead of micro/macro-scale carbon (graphite) powder?

“The carbothermal reduction of silica into silicon requires the use of temperature well above the silicon melting point (≥ 2,000 °C)”

Nagamori, M. *et al. Metail. Trans. B* **1986**, *17*, 503.
Zhihao, B. *et al. Nature* **2007**, *446*, 172.

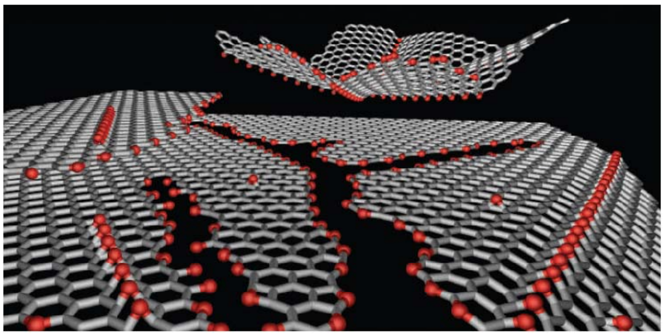
Small Amount of Oxygen : The Accelerator of SiO_2 Reduction

MATERIALS SCIENCE

Oxygen breaks into carbon world

Pulickel M. Ajayan and Boris I. Yakobson

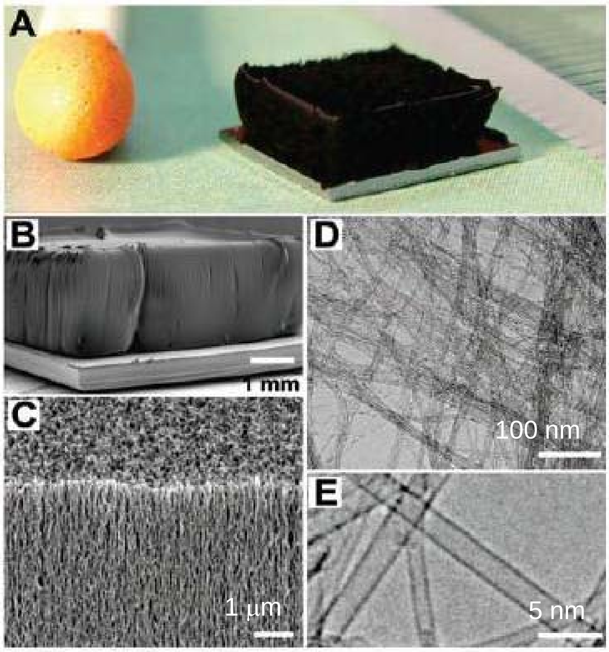
When oxygen atoms bind to a graphite surface, they fall into line and make bridges across carbon atoms. This is the spearhead of a chemical attack in which the atomic arrangement of solid carbon is torn apart.



Li, J. -L. et al. *Phys. Rev. Lett.* **2006**, *96*, 176101.
Ajayan, P. M. et al. *Nature* **2006**, *441*, 818.

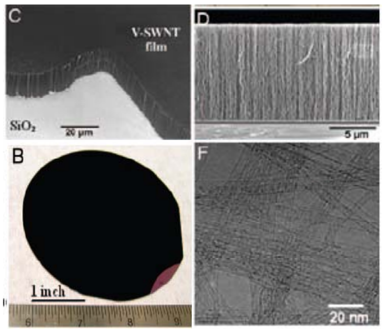
Oxygen-assisted CVD Growth of SWNTs : Increased yields - Vertical SWNTs on a substrate!!

H_2O vapor



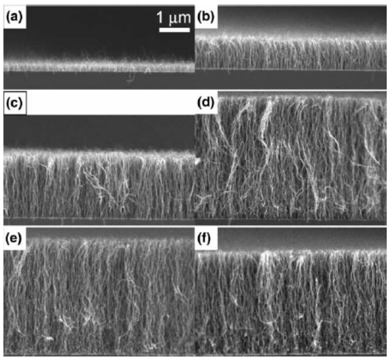
Hata, K. et al., *Science* **2004**, *306*, 1362.

O_2 gas
PECVD



Zhang, G. et al., *PNAS* **2005**, *102*, 16141.

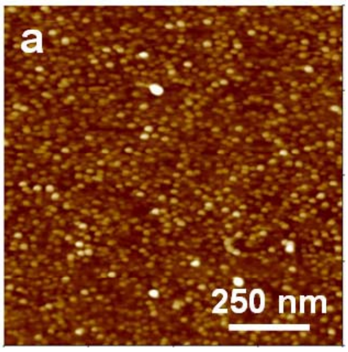
Ethanol vapor
10 Torr



Maruyama, S. et al., *Chem. Phys. Lett.* **2005**, *403*, 320.

The Oxygen effect on the SiO_2 etching using SWNTs

$FeCl_3 + NH_2OH$

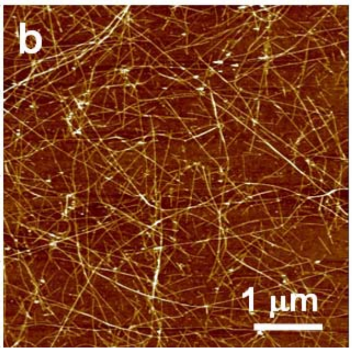


(a) Fe catalysts

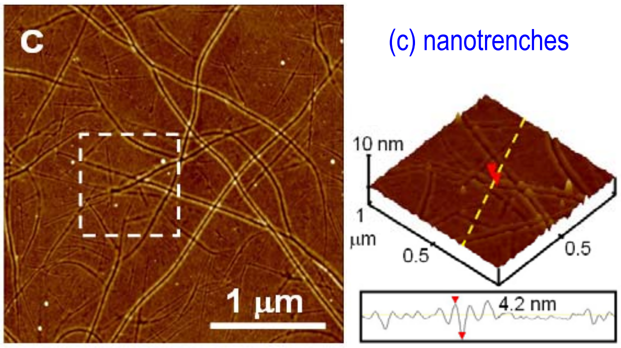
$H_2/CH_4/C_2H_4$

CVD
900°C 10 min

$H_2/CH_4/C_2H_4$
& O_2 (0.1 %)

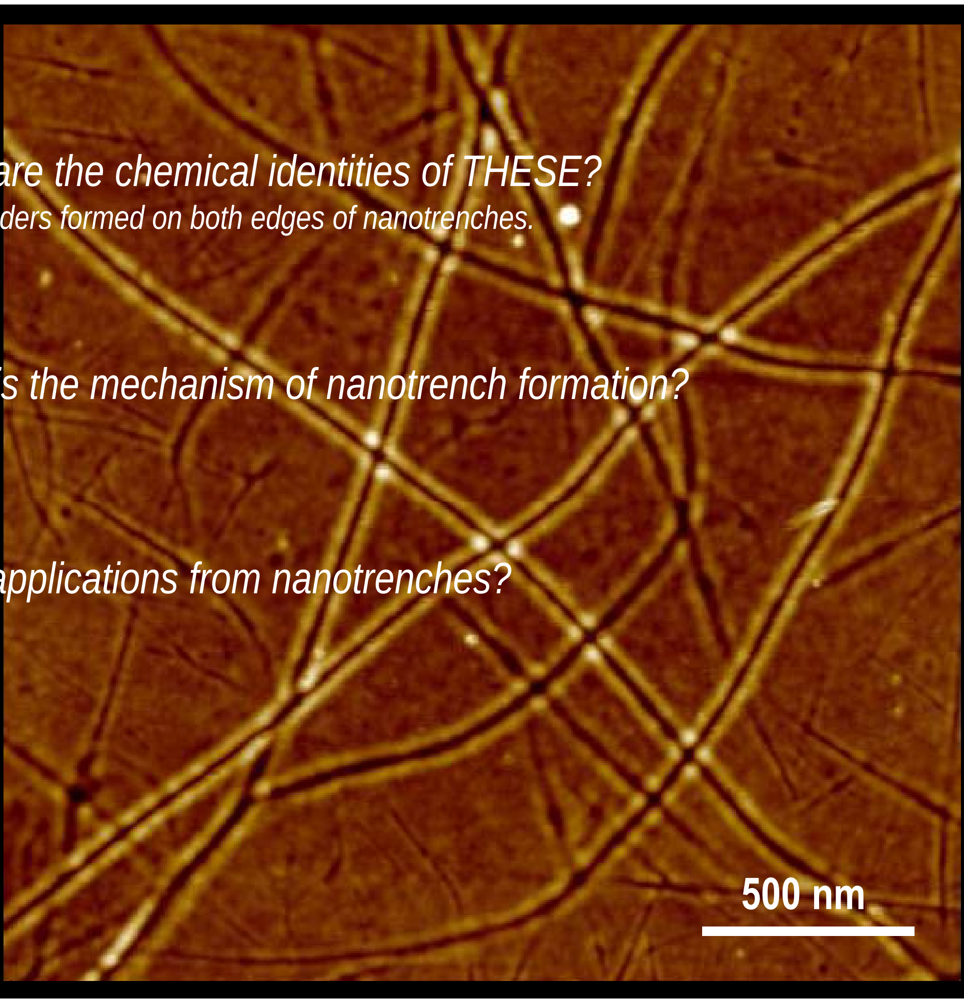


(b) SWNTs



(c) nanotrenches

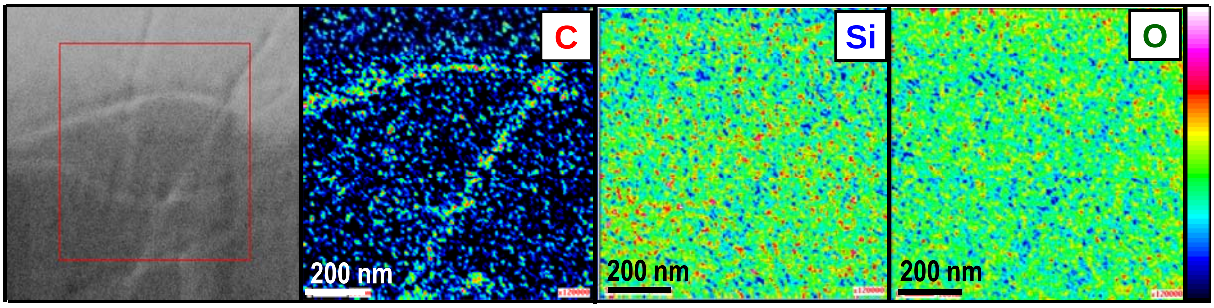
Byon and Choi *Nature Nanotech*. **2007**, *2*, 162.



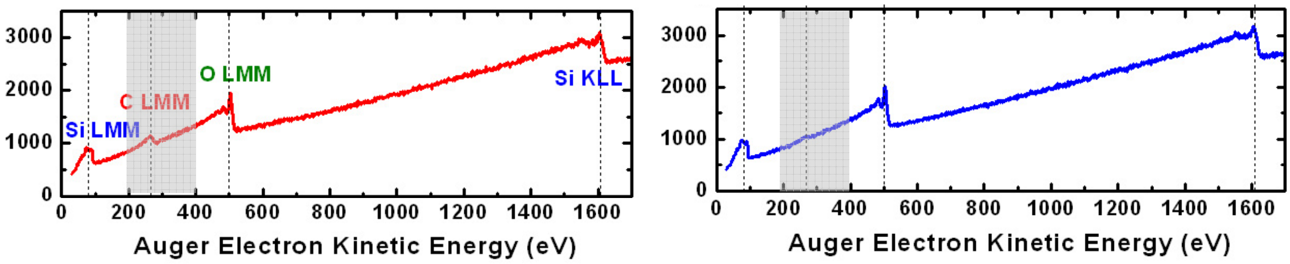
- *What are the chemical identities of THESE?*
  Shoulders formed on both edges of nanotrenches.
- *What is the mechanism of nanotrench formation?*
- *What applications from nanotrenches?*

Analysis of Nanotrench Shoulders : SEM/SAM images and AES Data

SEM & Scanning Auger Microscopy images



Auger Electron Microscopy measurement

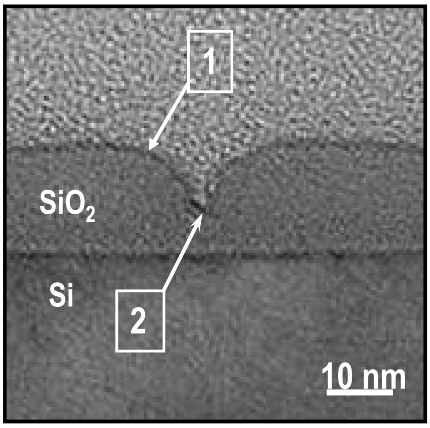


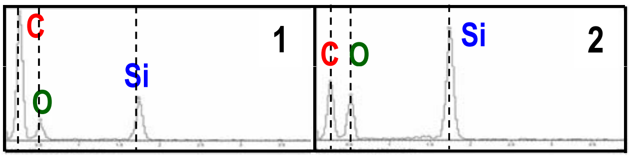
on the line

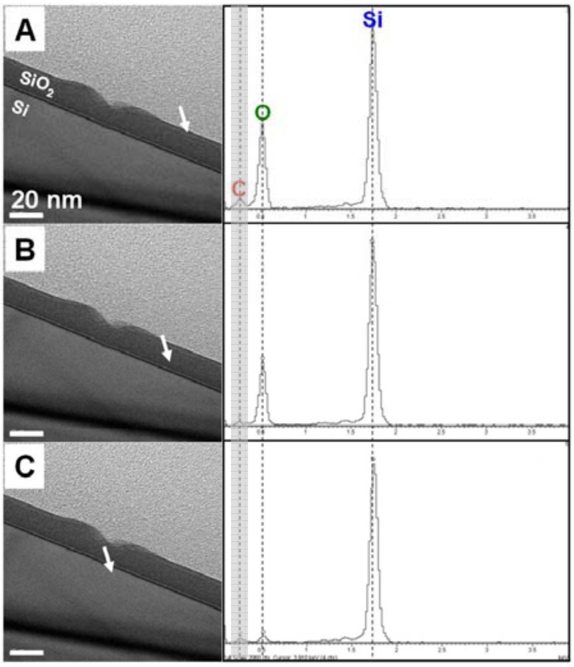
away from the line

Analysis of Nanotrench Shoulders : Cross-sectional HRTEM Images and EDX

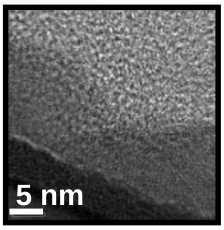
- average width by FWHM ~ 9.8 ± 2.4 nm
- average depth ~ 4.9 ± 1.9 nm

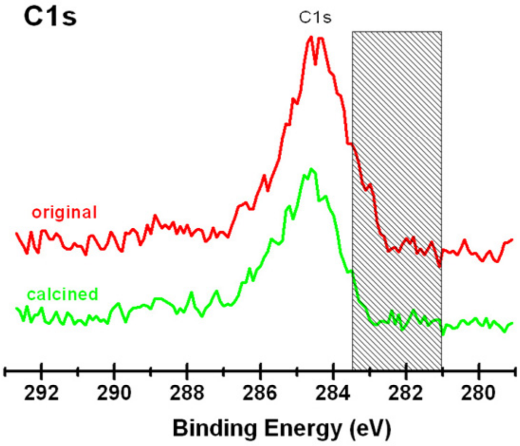


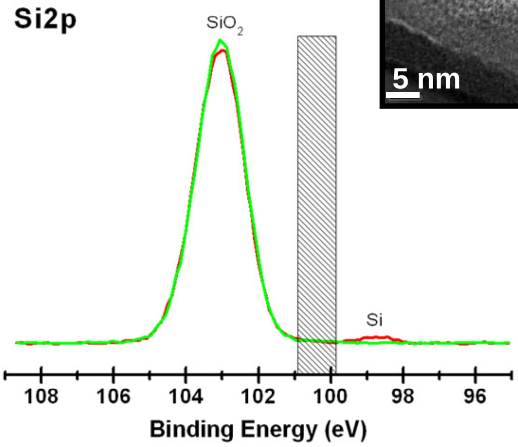




Analysis of Nanotrench Shoulders : XPS Spectra & HRTEM image





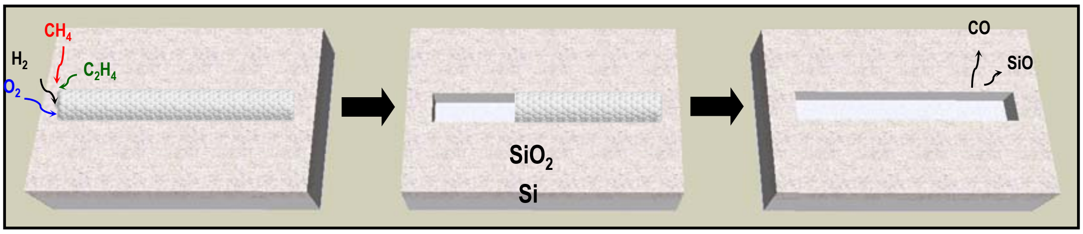


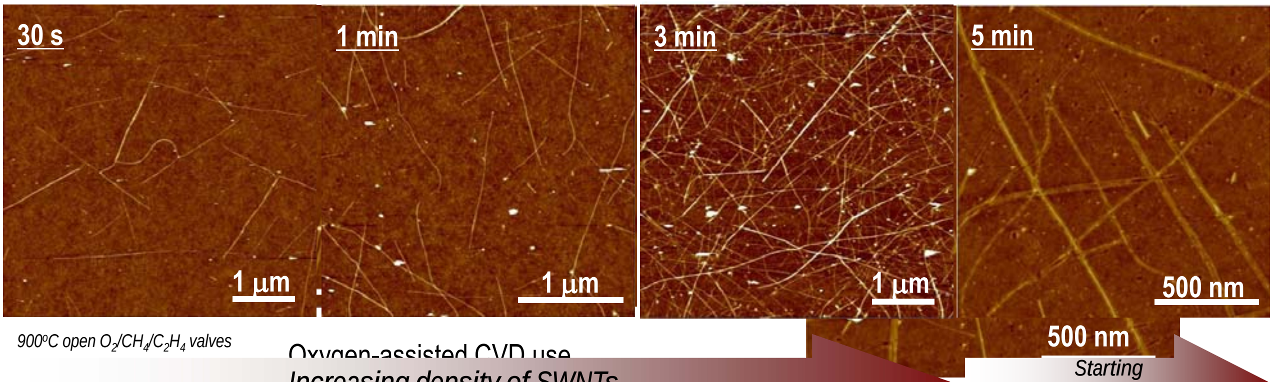
▨ Silicon carbide (SiC) peak range

→ *Amorphous SiO_2 with randomly deposited amorphous carbons*

$SiO(g) + ½ O_2(g) \leftrightarrow SiO_2(s)$

Carbon of SWNTs : The Precursor of SiO_2 Reduction





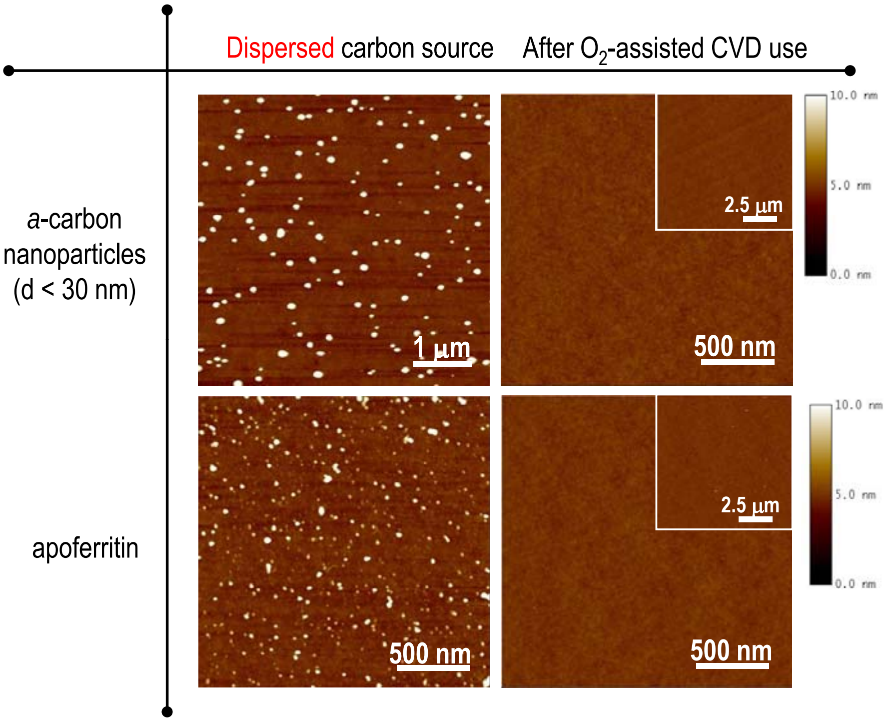
900°C open $O_2/CH_4/C_2H_4$ valves

Oxygen-assisted CVD use

Increasing density of SWNTs

Starting carbothermal Reduction

Carbon Effect (Carbon Nanoparticles without Fe catalyst)



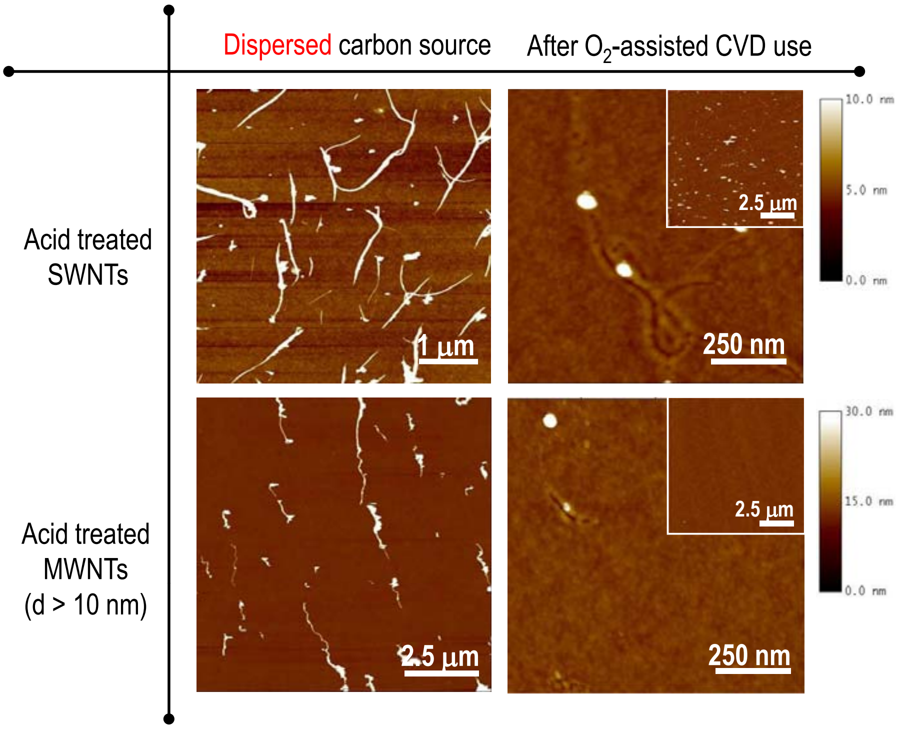
Dispersed carbon source

After O_2-assisted CVD use

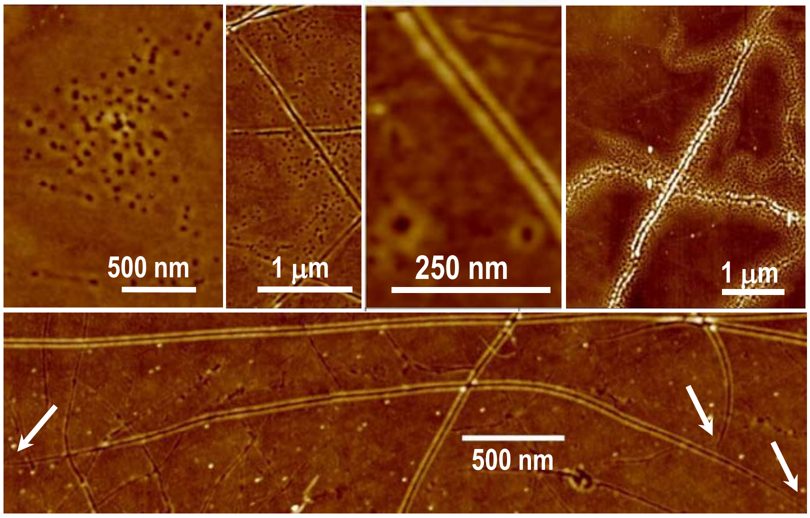
a-carbon nanoparticles (d < 30 nm)

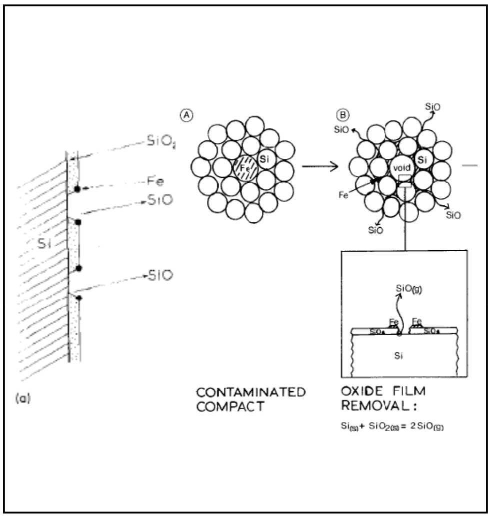
apoferritin

Carbon Effect (Carbon Nanotubes without Fe catalysts)

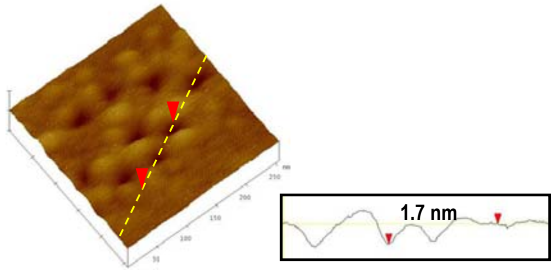


Fe Catalysts Removal: The Initiator of SiO$_2$ Reduction





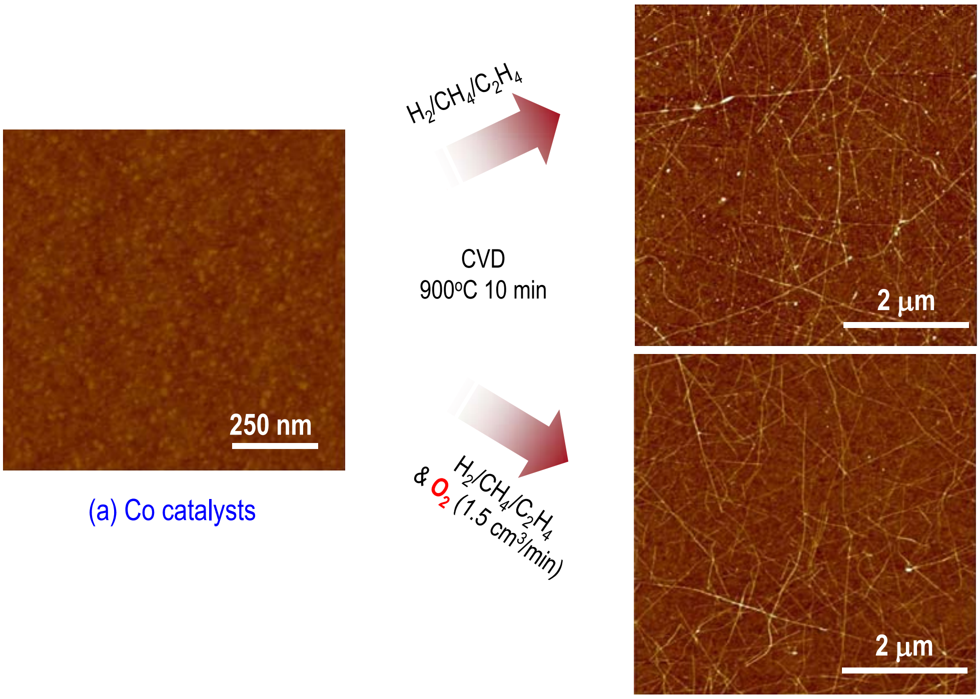
Moulson, A. J. et al. *J. Mat. Sci.* **1979**, *14*, 1017.
Boyer, S. M. et al. *J. Mat. Sci.* **1978**, *13*, 1637.



Co Catalyst Effect : No Nanotrench Formation

Soaking into cobalt acetate tetrahydrate ($(C_2H_3O_2)_2Co{\cdot}4H_2O$) 0.01 wt% in ethanol for 10 min
then calcination 400 °C for 5 min

Murakami, Y. et al. *Chem. Phys. Lett.* **2004**, *385*, 298.
Maruyama, S. et al. *Chem. Phys. Lett.* **2005**, *403*, 320.



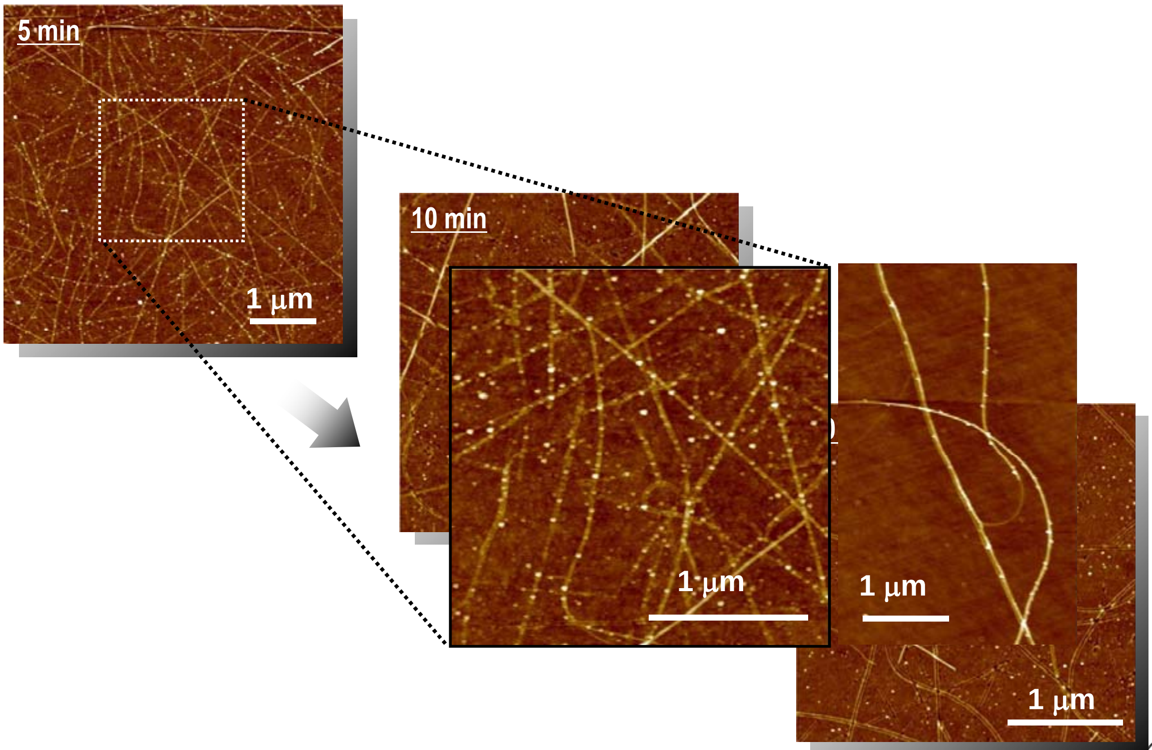
(a) Co catalysts

(b) SWNTs

(c) SWNTs (O_2-assisted CVD)

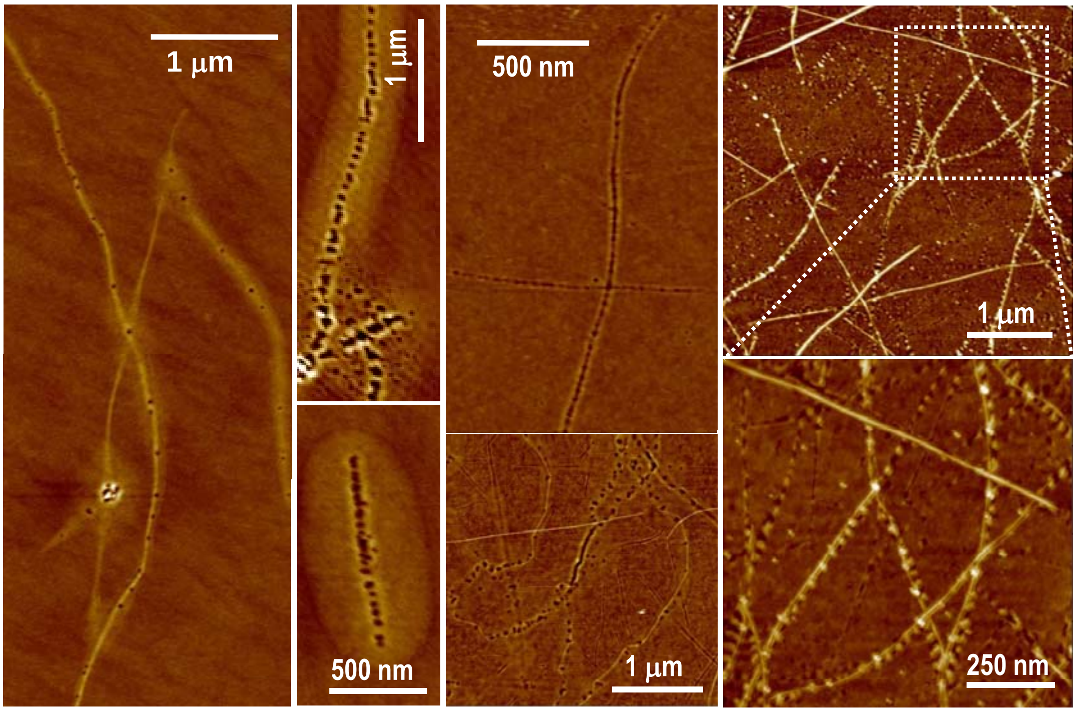
Self-Assembled Fe Catalysts on SWNT/SiO_2 Mechanism of Nanotrench formation?

900°C open $O_2/CH_4/C_2H_4$ valves

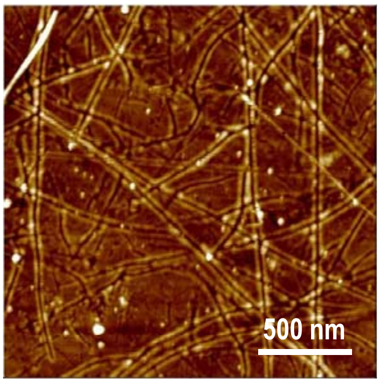


Byon and Choi *Unpublished results*

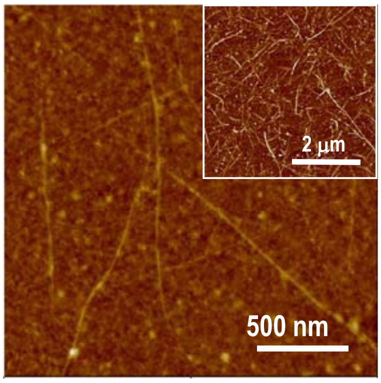
Removal of Self-Assembled Fe Catalysts on SWNT/SiO_2



Substrate Effect on the Carbothermal Reduction



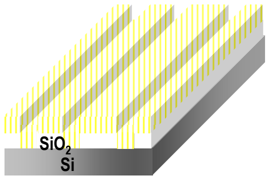
Quartz wafer
(crystalline SiO_2)



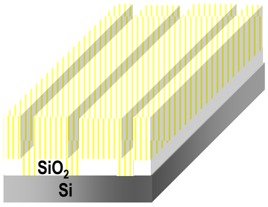
Si_3N_4 wafer

Applications of SiO$_2$ Nanotrenches : Cr Nanowires

target thickness : 4 nm



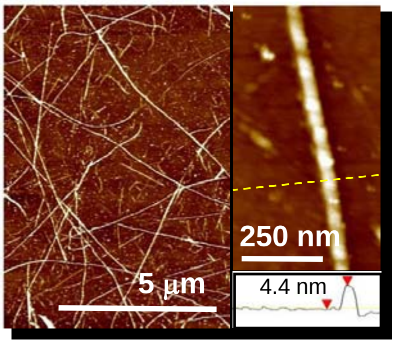
target thickness : 8 nm



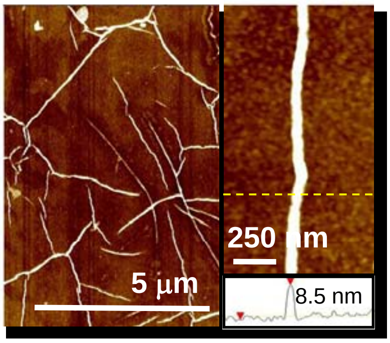
Cr Deposition
by using thermal evaporator

Lift-Off
by using 15% HF sol'n

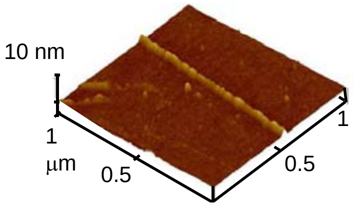
Cr Nanowires

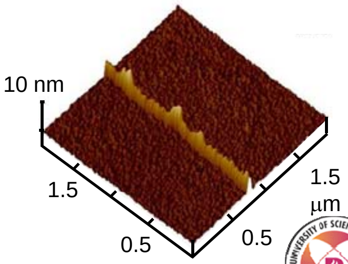


Avg. 4.4 ± 0.9 nm

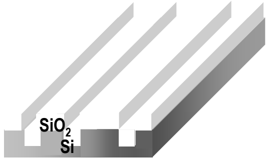


Avg. 10.4 ± 3.0 nm





Applications of SiO$_2$ Nanotrenches : Si Nanotrenches



Si etching
by using 45% KOH sol'n
(83 °C for 1 min)

Removal of SiO$_2$ mask
by using 15% HF sol'n