Solar Cell Market, Technology, & Activities of TES

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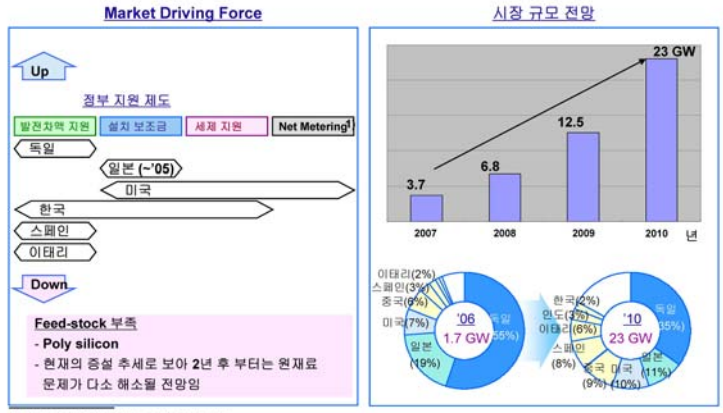
1. Introduction

PV Market Size

◆ **Kyoto Protocol** 실행안으로서 각국 정부의 지원제도,에너지/환경 정책에 힘입어 급속한 시장 성장을 예상하고 있음(이에 따라 현재 **Feed-Stock**(원재료) 부족 문제를 겪고 있음)

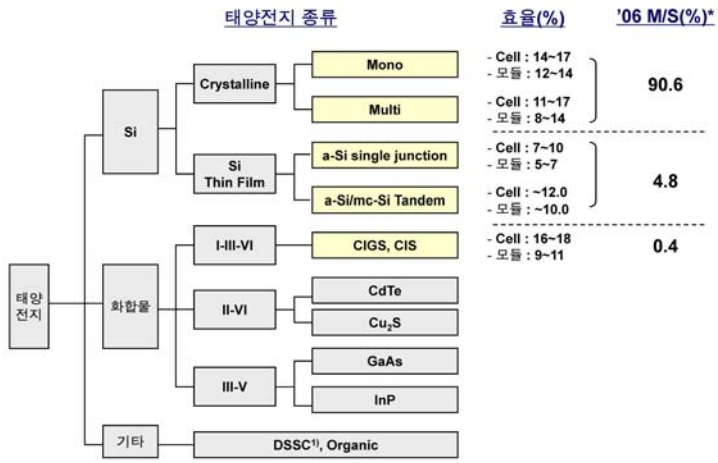


1) 발전 전력을 자체 소비 후 남은 전력 판매

1. Introduction

태양전지의 종류

❑ Solar cell은 Si계와 화합물계로 크게 대별되며, 현재 Market의 대부분은 Si계가 차지하고 있음
❑ Cell → Module 효율 loss : Crystalline < Si thin film < CIGS



1) DSSC : Dye sensitive solar cell
* Source : '08년 후지 키메라 종합연구소

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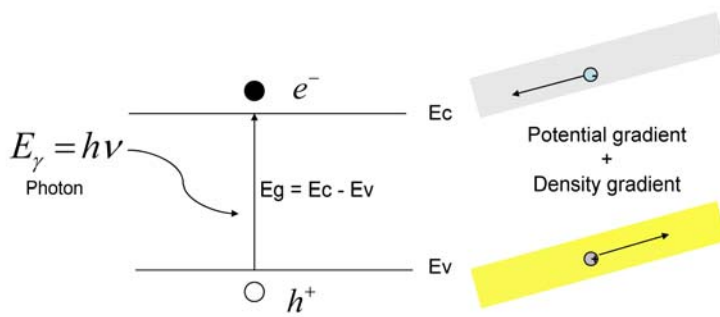
1. Introduction

원리 [1/2]

❑ 광전효과 (Photovoltaic effect)
: 광 에너지에 의해 전자와 홀이 생성되고, 유기된 전위차에 의해 전류가 발생하는 현상



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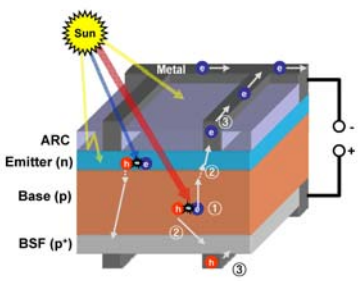
1. Introduction 원리 [2/2]

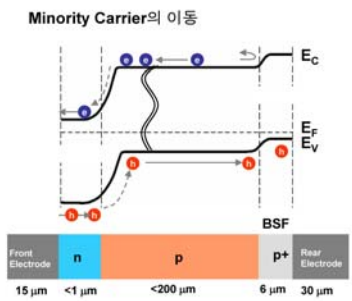
❑ 태양전지 : 빛을 전기로 직접 바꾸어 주는 전자소자 (광전소자, Photovoltaic device)

Step 1 : 광흡수에 의한 **electron-hole pair** 생성 ①

Step 2 : Minority carrier의 **diffusion**과 **drift**에 의한 이동 ②

Step 3 : Carrier 수집 ③

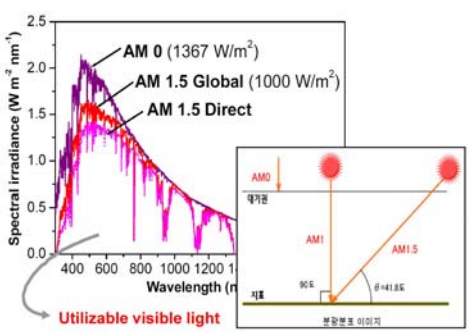


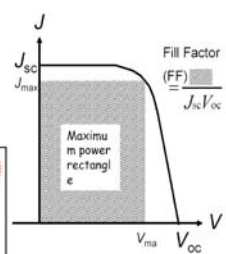


ARC : Anti-reflection coating
BSF : Back surface field

1. Introduction 주요인자

❑ **Standard test condition**에서 광량은 **1000 W/m² @25℃ (AM1.5)** 임
❑ 태양전지의 효율을 높이기 위해서는 **Jsc, Voc,** 및 **FF**의 개선이 중요함





AM (Air Mass) = $\frac{1}{\cos\theta}$

η(Solar efficiency) = $\frac{P_{max}}{P_s} = \frac{FF \times J_{sc} \times V_{oc}}{P_s}$

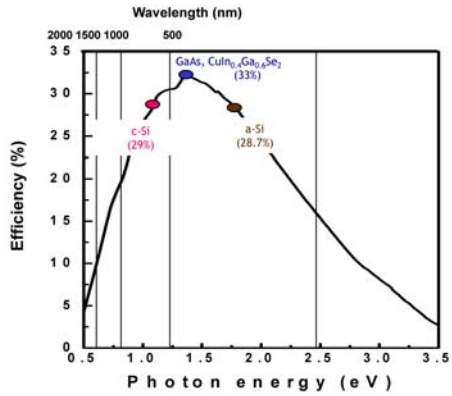
Jsc : Short circuit current Voc : Open circuit voltage
FF : Fill factor

1. Introduction

Ideal Cell Efficiency

❑ 광학적 및 전기적 손실이 없다는 가정하에
- 이론 최고 효율은 Bandgap 1.4 eV 에서 33%임 (AM1.5 spectrum)

❑ Bandgap 1.4 eV에 해당하는 재료
- GaAs, $CuIn_{0.4}Ga_{0.6}Se_2$



6 / 25

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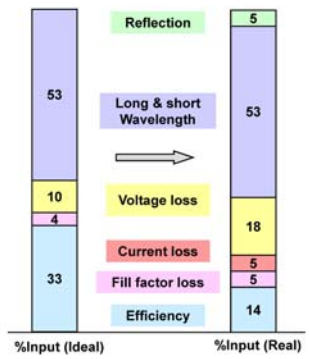
1. Introduction

Real Cell Efficiency

❑ Efficiency loss mechanism

실제효율



효율감소 내용

- **Reflection** : 표면에서의 반사
- **Long & short wavelength**
  : 장파장 - 에너지가 작아 전자-정공 쌍을 생성치 못함
  : 단파장 - 에너지가 커서 일부 열에너지 손실이 발생
- **Voltage loss**
  : **V (real) = V (ideal) - V_{drop}**
- **Current loss**
  : 물질 고유 특성 또는 결함으로 인하여 직렬저항, 병렬저항 존재
  → 전하의 생성과 수집확률이 따로 존재함
- **Fill factor loss**
  : 이상적인 **diode model**을 따르지 않음
  직렬저항, 병렬저항이 존재함

7 / 25

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1. Introduction

Efficiency Related R&D

	Factor	1st breakdown	2nd breakdown	Research Trends
빛을 효과적으로 흡수	Reflectance	반사감소	Anti-reflection Texturing	ARC (SiNx, Multi layer) Chemical texturing Dry texturing
		전면전극 감소	High aspect ratio Electrode area ↓	Hot-melt Back contact, Metal-wrap-through (MWT)
		후면반사 증가	Rear reflection	Back Surface Field (BSF) Back side passivation
전하를 효과적으로 생성	Bandgap Eng. Voc	넓은 파장대의 빛을 사용	장파장 +단파장	Multi junction Tandem structure
		Junction 특성 개선	Bandgap 증가	Hetero
전하를 효과적으로 분리	Jsc Fill factor	Recombination 감소	High life time Low defect (Surface, Bulk)	Gettering, Hydrogen passivation Forming gas annealing BSF, Rear local contact
전하를 효과적으로 수집	Jsc Fill factor	직렬저항 감소	Contact 저항 감소 Emitter 저항 감소	Buried contact Selective emitter
		누설 전류 감소	Shunt resistance ↑	Isolation (Laser, Wet, Plasma)

8 / 25

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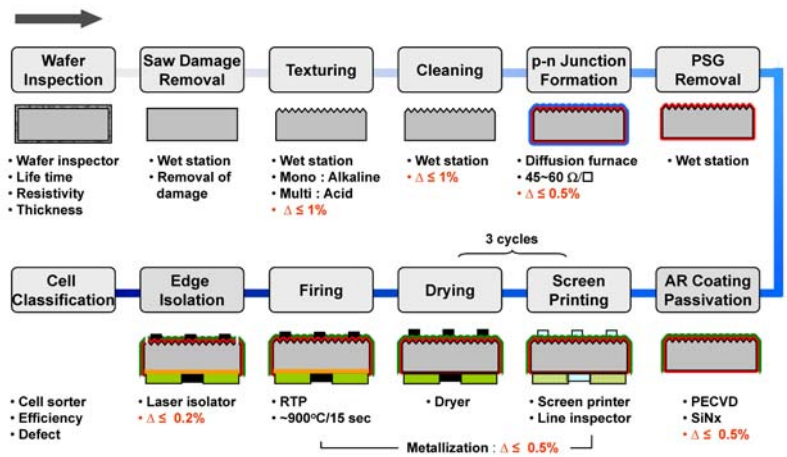
2.1 Crystalline Solar Cell

Fabrication Process

❑ 핵심공정의 기술 확보에 따라 최대 : **2~3%** 효율 편차 발생



PSG : Phosphorous silicate glass, AR: Anti reflection
RTP : Rapid thermal processing

9 / 25

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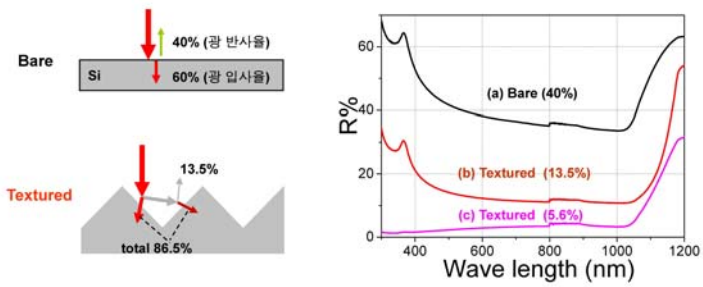
Texturing/ cleaning

Texturing | p-n junction | ARC | Metalli-zation | Edge isolation

❑ **Texturing (Δ≤1%): Si** 표면에 요철을 형성하여 빛의 반사를 최소화함
❑ **Cleaning (Δ≤1%): Si** 표면의 **ion**들을 제거하여 **recombination site** 제거



10 / 25

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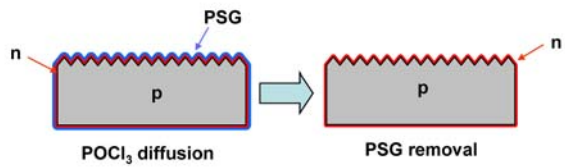
P-N junction formation

Texturing | p-n junction | ARC | Metalli-zation | Edge isolation

❑ **p type wafer**에 **n**형 원소**(P)**를 **diffusion**시켜서 **p-n junction**을 만드는 공정 (Δ≤0.5%)
: **wafer**를 **device**화 시키는 중요 공정
균일한 **sheet resistance (45~60Ω/□)** 제어→ 고효율



PSG : Phosphorous silicate glass

11 / 25

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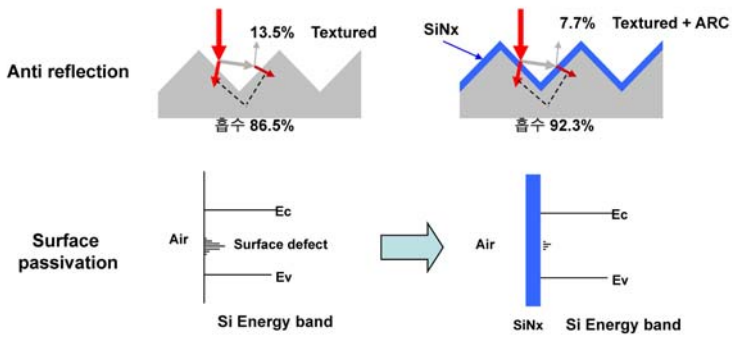
ARC & Passivation

Texturing | p-n junction | ARC | Metalli-zation | Edge isolation

❑ SiNx thin film (by PECVD) (△≤ 0.5%) : AR + passivation
- ARC : 입사되는 빛의 반사 억제
- Surface passivation : 표면의 dangling bond 전기적 결함 passivation

❑ 효율 향상을 위해 SiONx, SiOx/SiNx multilayer의 연구 등이 활발히 진행 중
❑ 굴절율 (2.0~2.3), 광투과도, Hydrogen 함량(>15%), Film density의 최적화 필요



ARC : Anti-reflection coating

12 / 25

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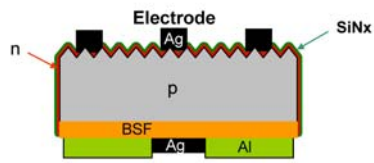
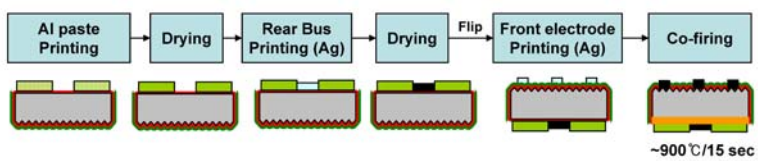
Metallization : Nominal

Texturing | p-n junction | ARC | Metalli-zation | Edge isolation

❑ 전면전극/emitter의 ohmic contact과 Al 확산에 의한 BSF 층 및 후면전극을 형성하여 소자를 전기적으로 완성시키는 중요한 공정 (△≤0.5%)
- Screen printing : 선폭, aspect ratio 중요, breakage rate 가장 높은 공정
- Drying : paste의 유기 binder를 제거
- Co-firing : Ag와 emitter의 electric contact 형성
  Al diffusion에 의한 BSF (p+ doping layer)형성





13 / 25

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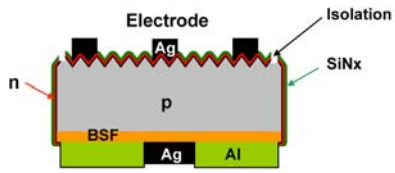
Edge Isolation

Texturing | p-n junction | ARC | Metalli-zation | Edge isolation

- ❑ Edge isolation (Δ≤ 0.2%): front/rear 절연을 통한 diode 형성
- ❑ Isolation 방법
  - Laser isolation : throughput이 높음



14 / 25

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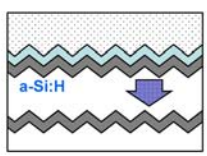
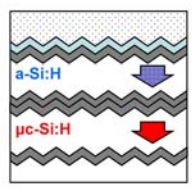
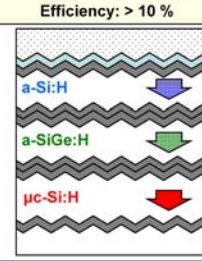
2.2 Si Thin Film — Overview

- ❑ Si shortage 및 제조원가 관점에서 박막 투자 확대
  - 2007 년 Turnkey 수주 규모 : 817 MW (Oerlikon - batch, AMAT- cluster, Ulvac - in line)
  - 제조비용 : 1.7 $/Wp (Crystalline : 2.5 $/Wp)
  - 초기 투자 비용이 큼 : 1.2~1.4 M$/MWp (Crystalline : 0.75~0.8 M$/MWp)
- ❑ Single junction cell이 주류이고 최근 Sharp에서 Triple junction cell의 생산을 시작했음

Single junction cell	Tandem (double junction) cell	Triple junction cell
Efficiency: 6~7 %	Efficiency: 9~11 %	Efficiency: > 10 %
		
Mass Production Stage		
- Japan: Kaneka - US: EPV - EU: Ersol, Schott Solar	Kaneka Mitsubishi Heavy Ind.	Sharp

15 / 25

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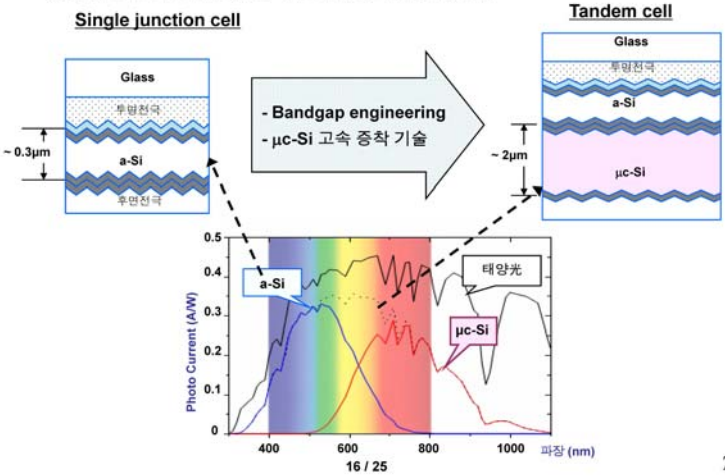
2.2 Si Thin Film 원리

❑ **a-Si (1.75eV)**과 **μc-Si (1.1eV)** 박막의 **Bandgap** 차이를 이용한 태양광의 분할 흡수로 효율 향상
❑ **Current matching**을 위해 상대적으로 두꺼운 **μc-Si** 박막이 필요함
→ 경제성 확보를 위해서는 **μc-Si** 박막의 고속 증착 기술이 필요함



16 / 25

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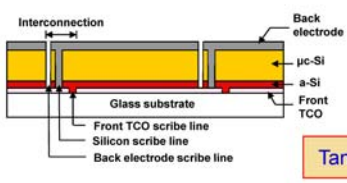
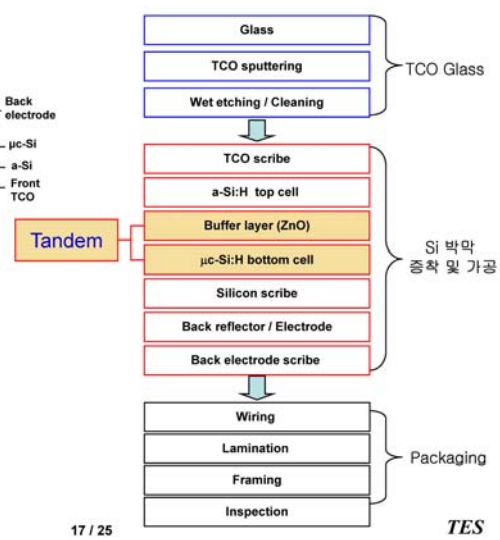
2.3 Si Thin Film Module 제조 공정

❑ 공정 장비가 LCD 장비와 유사
- **Glass** 기판
- **PECVD, Sputter**



Superstrate 구조



17 / 25

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TES
Technology Engine of Science
CHALLENGE
CREATE & CHANGE

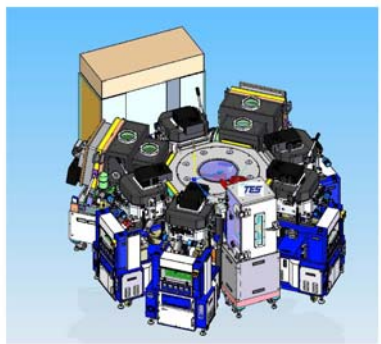
Total R&D Solution for Solar Cell

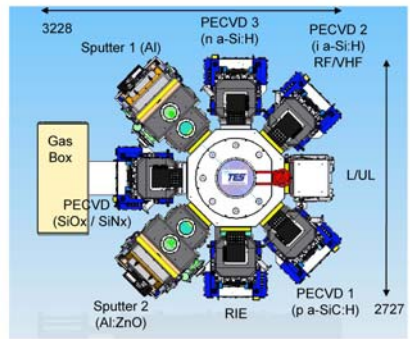
TES Solar Biz. Div.

Total R&D solution of solar cell investment

❑ **Deposition System for Total R&D Solution**

- **a-Si single junction cell**
- **a-Si/μc-Si double junction (tandem) cell**
- **Conventional bulk solar cell: Anti-reflection layer (SiNx), Dry texturing cell**
- **High efficiency bulk solar cell: Selective emitter cell, Double AR cell**
- **Hetero junction cell: Bulk + a-Si:H (ex. HIT cell of Sanyo, Japan)**

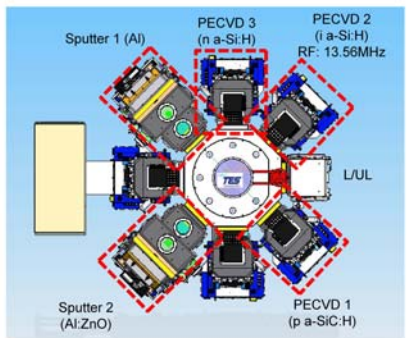




19 / 25

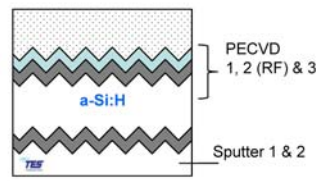
TES

1. a-Si single junction cell



● **Process Procedures**

-TCO Glass → PECVD 1 → PECVD 2 (13.56MHz)
→ PECVD 3 → Sputter 1 → Sputter 2



+ Laser (Scriber + Trimmer)

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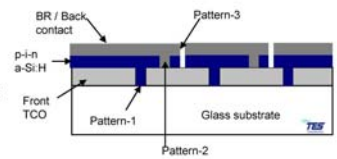

20 / 25

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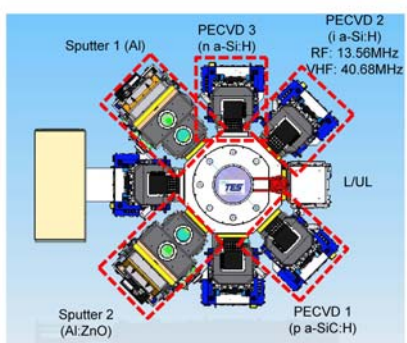
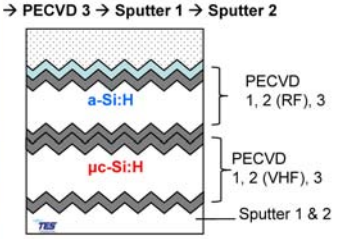
2. a-Si / μc-Si double junction (tandem) cell



● **Process Procedures**

-TCO Glass → PECVD 1 → PECVD 2 (13.56MHz)
→ PECVD 3 → PECVD 1 → PECVD 2 (40.68 MHz)
→ PECVD 3 → Sputter 1 → Sputter 2



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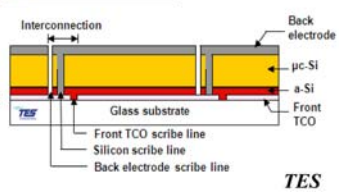

21 / 25

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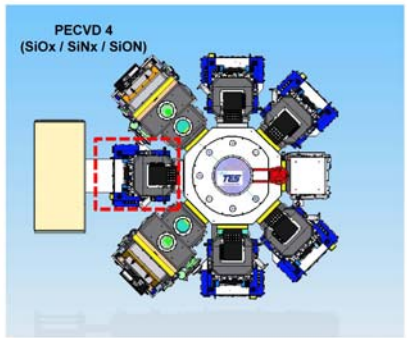
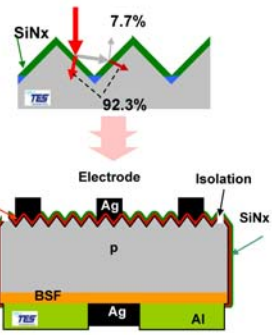
3. Bulk solar cell: Anti-reflection layer (SiNx)



- Single Anti-reflection
: Si_3N_4 (n~1.9), SiN (n~2.3), SiO (n=1.8~1.9), SiO_2 (n~1.46) and SiON (~1.9)
- Double Anti-reflection
: SiOx/ SiNx

● Key parameter

- Reflective index matching (n=1.9~2.0)
- Thickness matching (~80 nm)
- Surface passivation (Hydrogen contents)



22 / 25

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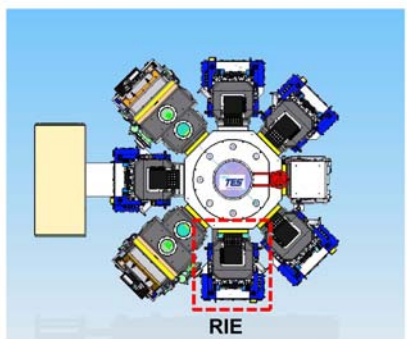
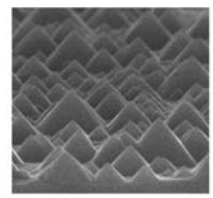
4. Bulk solar cell: Dry texturing

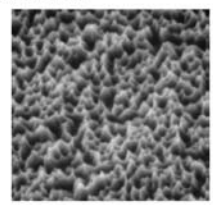


• Extra low reflectance
: High Jsc
: ex. Kyocera process

● Wet texturing



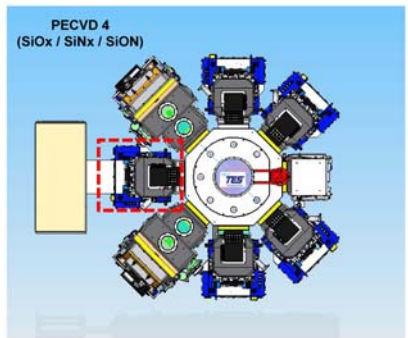
● Dry texturing



23 / 25

TES

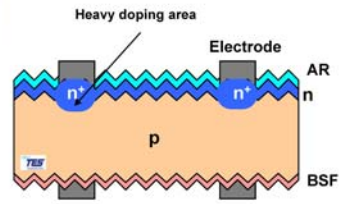
5. Bulk solar cell: selective emitter application



Selective emitter cell
(Thermal damage free phosphorous diffusion barrier)

- **Process Procedures**

- Wafer texturing → Diffusion barrier deposition → Oxide patterning (laser) → Diffusion →→→



\+ Laser
(Scriber + Trimmer)

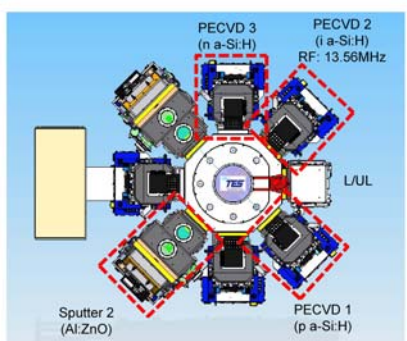
- Blue wave response improvement
: High Jsc & FF
: European trend

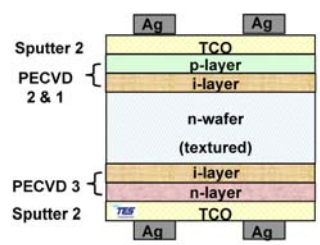
24 / 25

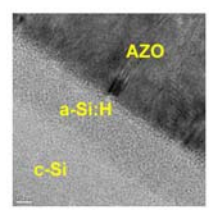
TES

5. Bulk solar cell: Hetero junction cell

- **Bulk + a-Si:H (ex. HIT cell of Sanyo, Japan)**
(Efficiency: ~22%)







25 / 25

TES