Polymer insulator patterning for multi-level metal interconnection in organic integrated circuits using iCVD

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Metal interconnect formation through multi-level structure is crucial technology for fabrication of integrated circuits (ICs). In organic electronic devices, however, it has been a technical hurdle to implement multi-level interconnection using conventional lithography due to insufficient chemical robustness of the organic material, which impedes higher degree of integration of organic circuits with multi-level structures. To overcome this issue, two matters should be settled. Firstly, deposition of insulating layer on the organic semiconductor without any damage on it, and secondly, patterning of the insulating layer to form interconnects between layers. Here, we present an interconnect scheme using patterned polymer insulator based on initiated chemical vapor deposition (iCVD). Patterning of insulating polymer layer while deposition via iCVD process excludes any solvents from entire fabrication process, thereby reducing the limitation on used of organic materials. We fabricated complementary organic circuits including inverter, NAND, NOR, and XOR with up to 3-level metal interconnect. The inverter showed high static gain (>170 V/V) and the logic gates were operated at VDD 10 V.