Simulation of charge-up coupled with universal surface reaction model in plasma process

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As the feature size in next generation device such as 3D memory and FINFET in semiconductor industry continues to decrease up to few nm level, plasma etching technology emerges one of the key bottleneck process. In nanoscale device fabrication abnormal profile such as twisting, bowing and etch stops is one of severest problems. Some researches pointed out that the abnormal profiles are caused by the distortion of the ion trajectory. To address these issues in this work, we developed a 3D charge-up model which could be incorporated into 3D feature profile simulator named as K-SPEED. Charge-up simulation was composed of ion transport module and 3D Poisson equation. Furthermore, the universal plasma surface reaction model developed over the years was strongly coupled with this charge-up simulation using 3D topography simulator. So, we can confirm the phenomenon of charge-up effect under the realistic steady state passivation layer. Finally, we demonstrated that this work can explain the unveiled charge-up effects during plasma etching of nanoscale feature.