광도파로 소자의 패키징 기술

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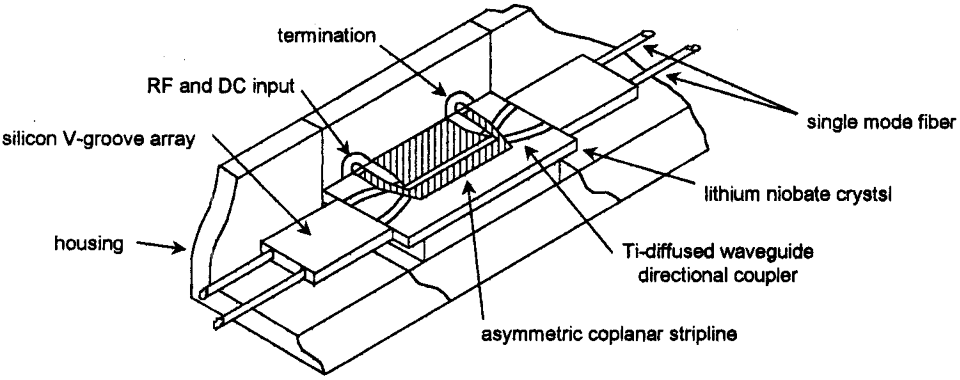
Contents

- Introduction
- Fiber Block
- Pigtailing *(optical)*
- Housing *(electrical / mechanical)*
- Reliability Test
- Advanced Packaging Techniques
- Summary

Introduction
What is "Guided-Wave Device Packaging" ?

chip dicing → polishing → test
fiber block fabrication → polishing → test
→ pigtailing → housing → reliability test



Packaging Issues

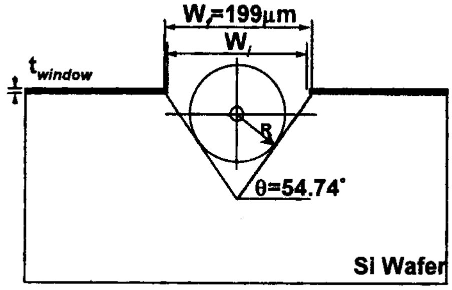
- Physical size or geometry issues
- Material issues
- Mechanical / thermal issues
- Electrical issues (TO, EO Devices)
- Optical issues
- Assembly issues

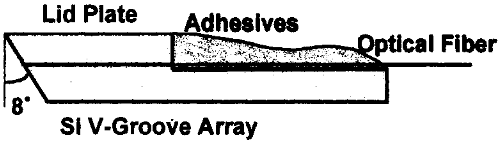
→ **Reliability, Manufacturability, Low cost**

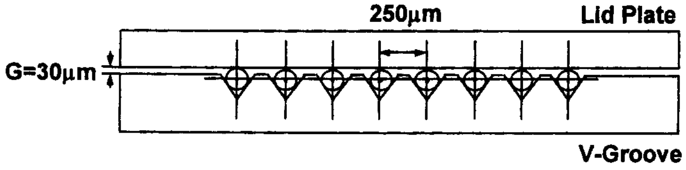
Comparison of Guided-Wave Devices

	$LiNbO_3$	Silica	Silicon	III - V (InP)	Polymer
Operating Windows · 830nm ·1310nm ·1550nm	·Yes ·Yes ·Yes	·Yes ·Yes ·Yes	·No ·Yes ·Yes	·No ·Yes ·Yes	·Yes ·Yes ·Yes
Refractive Index	2.2	1.45	3.4	4.0	1.5
Propagation Loss	≤0.5dB/cm	≤0.05dB/cm	≤0.1dB/cm	≤3.0dB/cm	≤0.1dB/cm
Fiber Coupling Loss	2.0dB/facet	0.3dB/facet	0.5dB/facet	7.5dB/facet	0.5dB/facet
Maximum Modulation	40GHz	1KHz	1KHz	40GHz	40GHz
Module Cost	High	Medium	Low	High	Low
Market Status	Commercialized			Prototype	

Fiber Block
Structure of Fiber Block





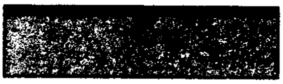


Method of V-Groove Formation

- ◆ Wet etching of Si wafer
  - etch rate difference between (100) and (111) surface
  - etchant: water solution of KOH *or* EDP
  - mask material: Si_3N_4 *or* SiO_2
- ◆ Machining with V-shaped diamond wheel
  - various material can be used for V-groove block
- ◆ Precision plastic molding
  - low cost method for mass production

V-Groove Fabrication Process: Si Wet Etching

1. Si_3N_4 sputtering ~1500 Å

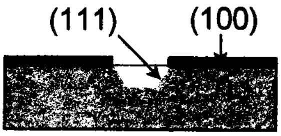


2. Photolithography

3. Si_3N_4 RIE

4. Strip photoresist

5. Si wet etching

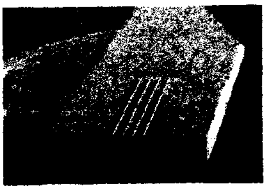


6. Final V-groove

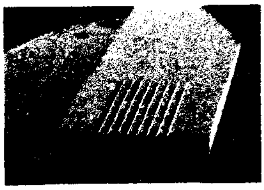
80℃ 40 wt% KOH: H_2O solution
etch ratio (100):(111) ~ 100:1

V-Grooves: Silicon Wet Etching

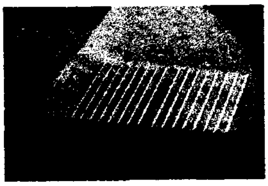
- ◆ V-groove cross section



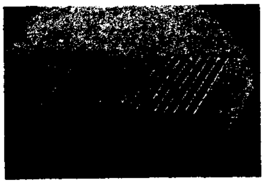
4F V-Groove



8F V-Groove



16F V-Groove



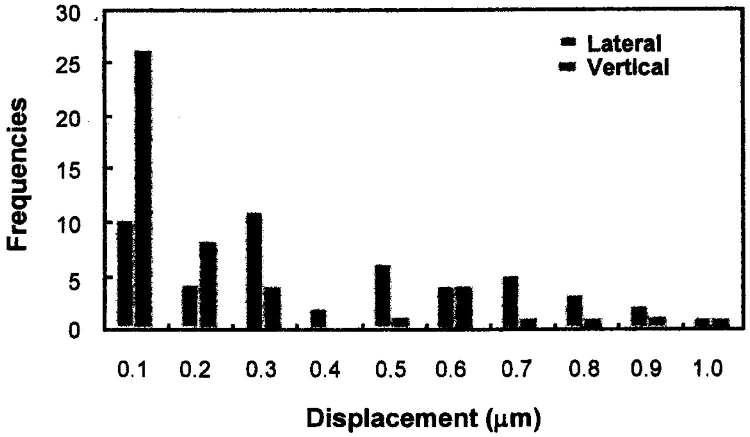
32F V-Groove

Fiber Block Uniformity

- ◆ **Average position error**

  ±0.41㎛ (Spacing Error)

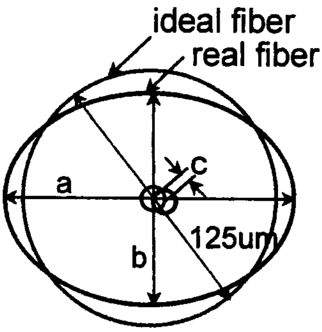
  ±0.24㎛ (Vertical Error)



Source of Fiber Position Variation

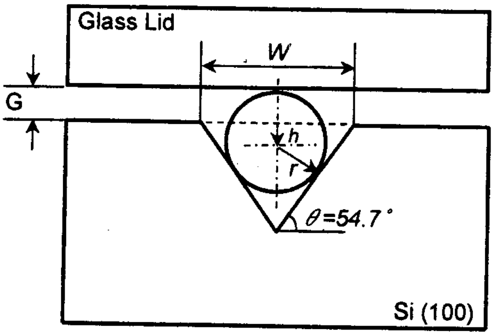
- Fiber characteristics
  - clad diameter: 125 ± 1 um
  - clad ovality : ≤ 1%

    $$\frac{a-b}{125}\times 100\%$$
  - mode field offset (c) : ≤ 0.8um



- Si lattice-to-mask misalignment
  - rough etching of (111) surface

Vertical Position Variation



- Fiber diameter error

$$\frac{dh}{dr}=\frac{1}{\cos\theta}\cong 1.7$$

MFD offset ≤ 0.5㎛
MFD variation ≤ 0.5㎛
Clad diameter 125.0±1.0㎛

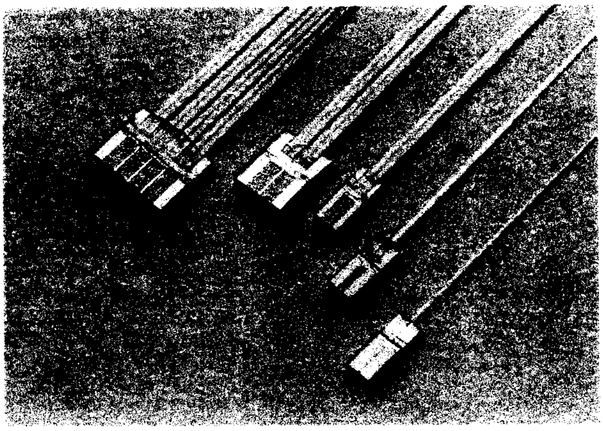
- Lithography error

$$\frac{dh}{dW}=-\frac{\tan\theta}{2}\cong -0.7$$

Fiber Block Characteristics

Number of Fibers	1, 2, 4, 8, 16, 32
Fiber Diameter	125μm
Fiber Spacing	250±1μm
Thickness of Silicon	1000±25μm
Height of Fiber Center	-32.5±10μm
Vertical Uniformity	±0.5μm
Temperature	-40 to +85℃

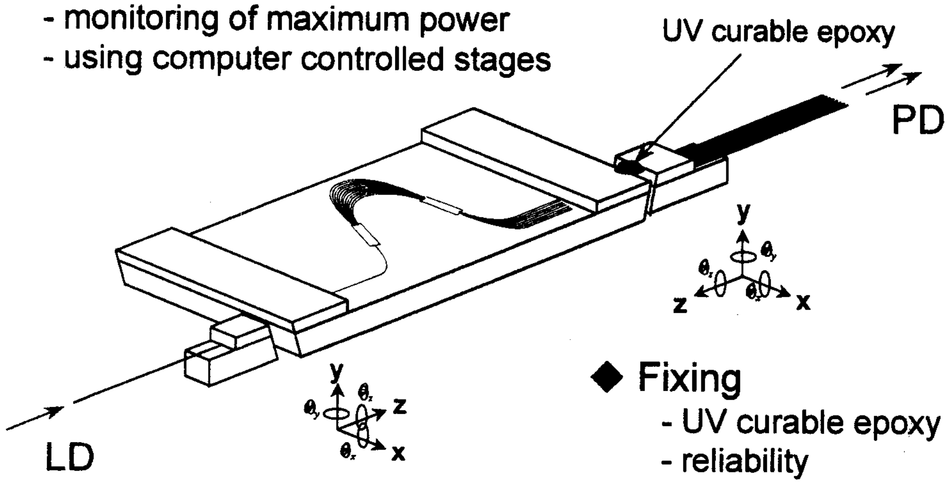
Photograph of Fiber Blocks



1, 4, 8, 16, 32F fiber block using Si V-grooves

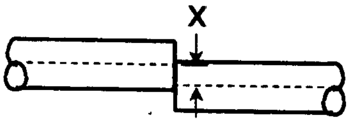
Pigtailing
Alignment and Fixing

- ◆ Active alignment
  - \- monitoring of maximum power
  - \- using computer controlled stages



- ◆ Fixing
  - \- UV curable epoxy
  - \- reliability

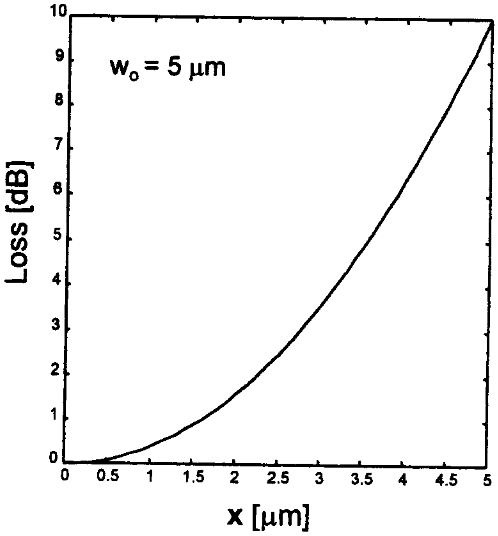
Loss Due to Lateral Misalignment



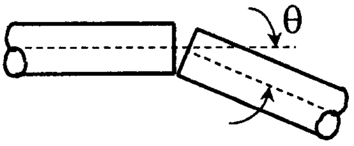
$$L_{lat} = -10 \log \left[e^{-U^2} \right]$$

where $U = \dfrac{X}{w_o}$

w_o: mode radius
at $1/e^2$ power density



Loss Due to Angular Misalignment



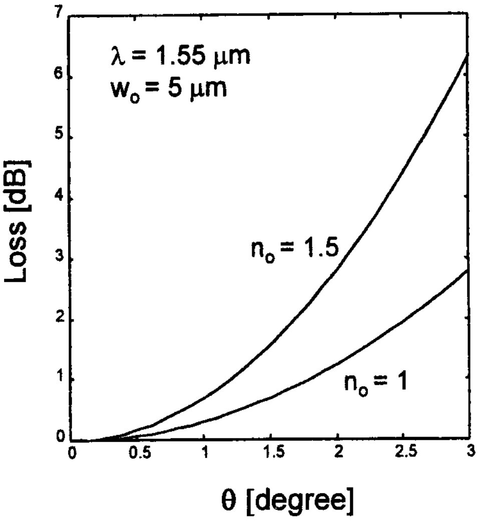
$$L_{ang} = -10 \log \left[e^{-T^2} \right]$$

$$\text{where} \quad T = \frac{n_o \pi w_o \sin\theta}{\lambda}$$

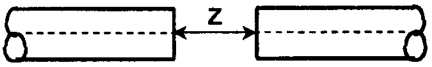
n_o: inter medium index

w_o: mode radius

at $1/e^2$ power density



Loss Due to Longitudinal Misalignment



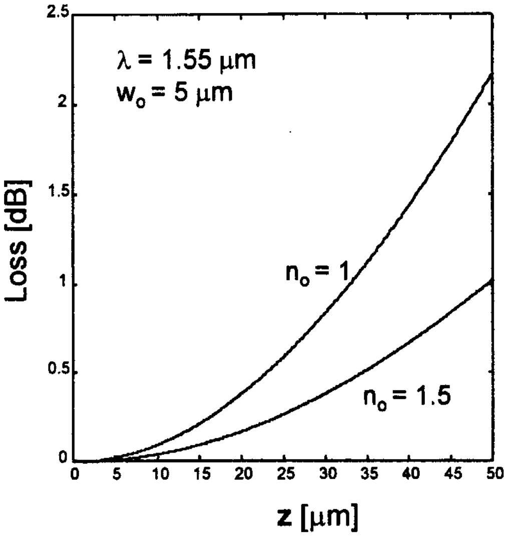
$$L_{long} = -10 \log \left[\frac{1}{Z^2 + 1} \right]$$

$$\text{where} \quad Z = \frac{z\lambda}{2\pi n_o w_o^2}$$

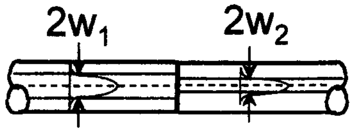
n_o: inter medium index

w_o: beam radius

at $1/e^2$ power density

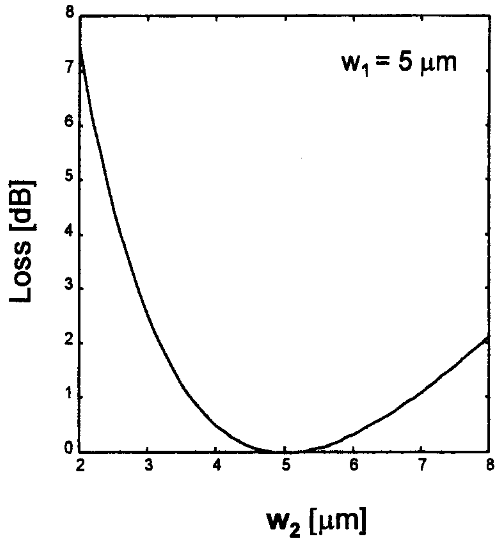


Loss Due to Mode Field Mismatch

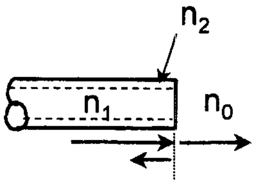


$$L_m = -10\log\left[\frac{4}{\left[\left(\frac{w_2}{w_1}\right)+\left(\frac{w_1}{w_2}\right)\right]^2}\right]$$

w_1 , w_2 : mode radius
at $1/e^2$ power density

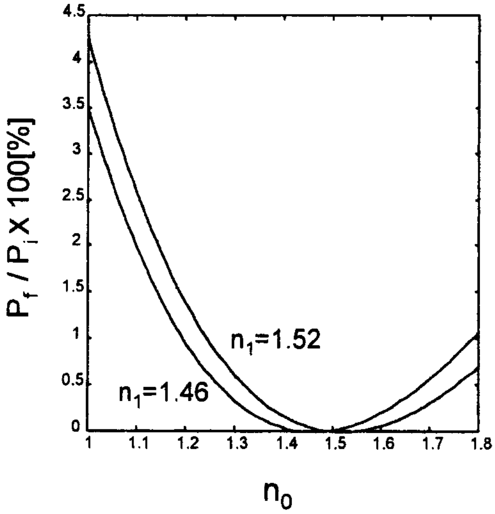


Fresnel Reflection Loss



$$P_f = \left[\frac{n_1 - n_0}{n_1 + n_0}\right]^2 P_i$$

P_f : reflected optical power
P_i : incident optical power
n_0 : inter medium index
n_1 : core index (fiber: ~1.46)



Required Properties of UV Curable Epoxy Resin

- Optical transparency: 0.5 ~ 1dB/mm (not critical)
- Refractive index matching: 1.45 ~ 1.7 (not critical)
- Viscosity: 100 ~ 500 cps
- Shrinkage during curing: < 2%
- High bonding strength
- Low CTE: $< 5 \times 10^{-5}/℃$
- Humidity / chemical resistivity

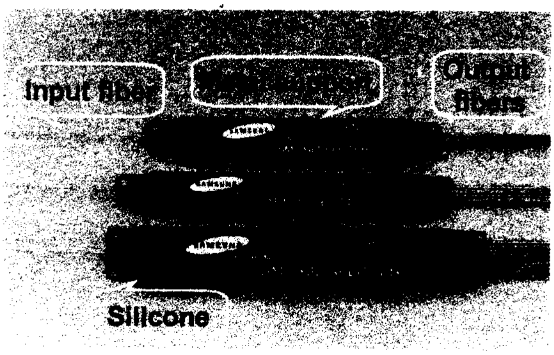
➔ **Reliable fixing** of guided-wave device chip and fiber block in spite of environmental change!

Housing
Consideration Point of Housing

- What kind of device?
  - passive *or* active device
  - temperature sensitivity of device characteristics
  - humidity durability of device (hermetic *or* nonhermetic)
  - driving electical frequency (active device)
- Materials for housing
  - metals, plastics, ceramics, silicone gel, etc.
  - CTE, themal conductivity, Young's modulus, electrical resistivity, etc.
- Reliability, Cost

Passive Device Housing
Optical Power Splitter

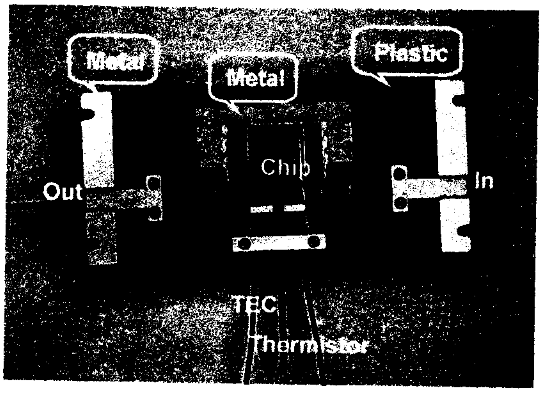
- ◆ SAMSUNG, 1XN splitter (N=8, 16, 32)
  - temperature insenstive device: no temperature control



- silicone resin molding
  - protection from humidity and mechanical shock
  - strain relief
  - low cost
- metal support
  - reinfocement of mechanical strength

Passive Device Housing
Arrayed Waveguide Grating

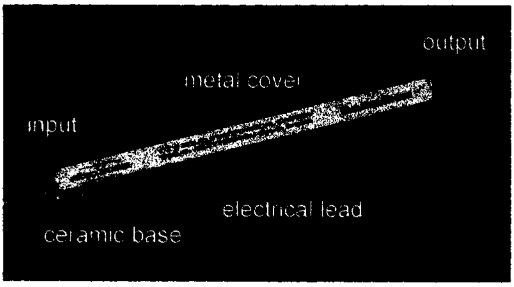
- ◆ SAMSUNG, WDM-DEMUX (8 channels)
  - temperature sensitive device: center wavelength change (0.011nm/℃)



- temperature control
  - using thermo-electric cooler and thermistor
- metal part
  - heat sink
- plastic part
  - thermal isolation

Active Device Housing
Thermo-Optic Switch

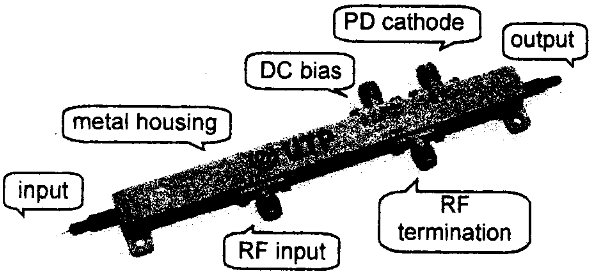
- ◆ AKZO, 1X8 optical switch
  - driving electrode (micro heater): electrical lead (~ms signal)



- hermetic package
  - high reliability
- electrical lead
  - switching signal
  - wire bonding to chip

Active Device Housing
Electo-Optic Device

- ◆ UTP, 10Gb/s digital modulator
  - driving electrode : ~GHz modulation signal, DC bias, etc.



- metal housing
  - EMI shielding
  - electircal ground
- electrical driving
  - impedance matching
  - RF transmission line

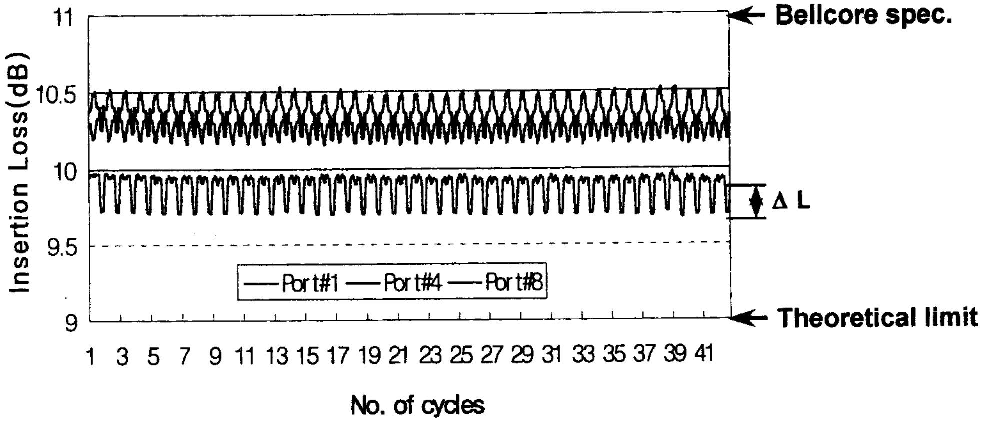
Reliability
Device Operating Conditions

Condition	Commercial	Rugged	Full Mil
Operating Temperature	0 to 55℃	-40 to 70℃	-55 to 85℃
Storage temperature	-55 to 85℃	-55 to 100℃	-62 to 125℃
Thermal Shock	±10℃/min	±20℃/min	±30℃/min
Humidity	0 to 95%	0 to 95%	0 to 100%
Vibration	5 to 100Hz, 2g	5 to 500Hz, 2g	5 to 2kHz, 10g
Shock	10g, 6ms	20g, 6ms	20g, 11ms

Typical Reliability Test Condition
Bellcore GR-1209

Temperature-Humidity Aging	Temp: +85±2℃, 336 Hours Humidity: 85±2%
Temperature-Humidity Cycling	Temp: +40±2℃ ~ +75±2℃, 336 Hours (14 Days, 8 Hour/Cycle) Humidity: 85±2% (+2℃ ~ +32℃) 80% ~ 10% (+32℃ ~ +75℃) Uncontrol (Below +2℃)
Water Immersion	pH: 5.5±0.5 Temp: +43±2 ℃, 168 Hours
Vibration	10 - 55 Hz, 1.52 mm Amplitude, for 2 Hours
Flex Test	1 lb Load, 100 Cycles
Twist Test	1 lb Load, 100 Cycles
Side Pull	0.5 - 1 lb Load, 90 Angle
Cable Retention	1.0 - 2.2 lb, for 1 Minute
Impact Test	6 ft Drop, 8 Cycles, 3 Axis

Temperature-Humidity Cycle Test: Silica 1X8 Splitter



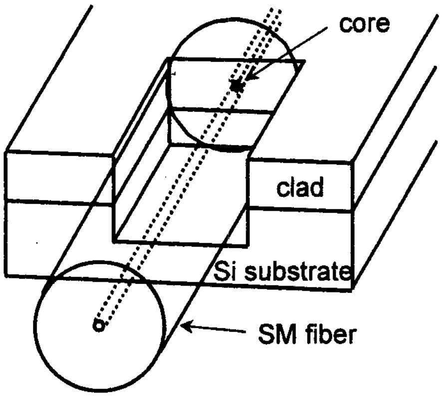
- Average insertion loss variation, ΔL= 0.248 dB (0.156~0.337dB)

Advanced Packaging Techniques Passive Alignment & Hybrid Integration

- Passive alignment (↔ Active alignment)
  - micromachined silicon waferboard substrates
  - complementary structures on platforms and devices
  - solder bump alignment forces (surface tension)
  - precision vision and accurate pick and place

- Hybrid integration
  - planar lightwave circuit (PLC) platform
  - integration of optical source (LD), optical detector (PD), thin film filter, etc.

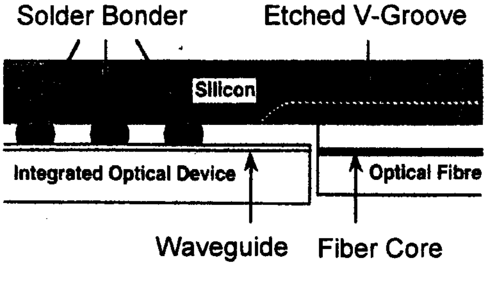
Etched Waveguide Groove Alignment



- passive alignment
- guiding grooves fabricated at the same time as waveguide
- < 0.4dB loss

– Yamada, et al, NTT, J. Lightwave Tech. 5, no 12, 1987

Solder Bump Self-Alignment



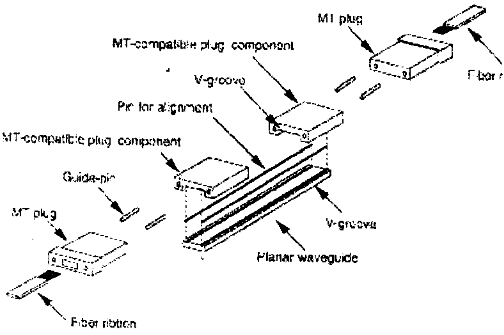
- Si V-groove platform
- wettable pad (Cr-Cu-Au) on Si platform and waveguide chip
- flip-chip coarse alignment
- self-alignment by solder reflow
- ~1 dB loss, LN / fiber

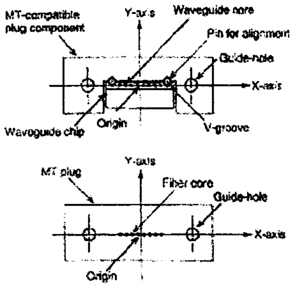
– M. J. Wale, Plessey, ECTC 1990, vol 1, pp. 34-41, 1990

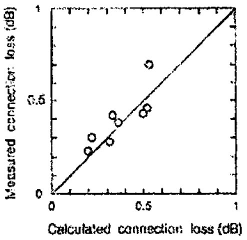
Solder Alloys

Solder Type	Comments
50 In / 50 Sn	118 ℃ Solidus - 125 ℃ Liquidus, Use for non-metals
52 In / 48 Sn	118 ℃ eut. Wets quartz, glass and some ceramics
In	Low T, 157 ℃
90 In / 10 Ag	141 ℃ -237 ℃, Stronger than In
80 In / 15 Pb / 5 Ag	Good solder against Au, low thermal fatigue
63 Sn / 37 Pb	183 ℃ eut. Wave solder at 200 -220 ℃
3.5 Ag / 96.5 Pb	221 ℃ eut. (do not use against Ag or Au)
80 Au / 20 Sn	280 ℃ eut. Wide application in OE device bonding
In with balanced Pb	Used for step temperature soldering
92.5 Pb / 5 In / 2.5 Ag	300 ℃ - 310 ℃, Very low thermal fatigue
5 Sn / 95 Pb	310 - 308 ℃, Wide application (do not use against Ag or Au)
80 Au / 12 Ge	356 ℃ eut.
40 Sn / 60 Pb	361 ℃ - 460 ℃, Common use against Cu parts

Waveguide Chip with MT-Compatible Plug Components

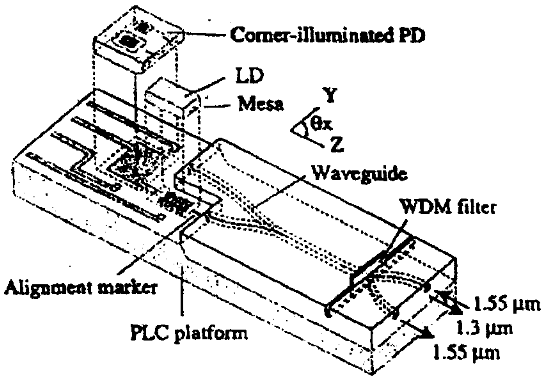






– **M. Takaya, et al, NTT, IPR 1996, IWH2, 1996**

Hybrid Integration with PLC Platform



- PLC platform
- marker alignment method: SS-LD, PD
- WDM filter (1.3/1.55 µm)
- optical network unit (ONU)

– G. Nakagawa, et al, Fujitsu, J. Lightwave Tech. 16, no 1, pp. 66-72, 1998

Summary

◆ Consider operating environmental condition, device characteristics, cost , etc.

➔ Decide package type, materials, etc.

◆ Packaging cost reduction

- pigtailing: active alignment → passive alignment
- discrete device → hybrid integration
- reduce the number of assembly parts
- use molding method for mass production